IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG DISPLAY CO., LTD., Plaintiff, v. AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; CHI MEI OPTOELECTRONICS CORPORATION, and CHI MEI OPTOELECTRONICS USA, INC., Defendants.	Civil Action No. 06-726 (JJF)
AU OPTRONICS CORPORATION, Plaintiff, v. LG DISPLAY CO., LTD. and LG DISPLAY AMERICA, INC., Defendants.	Civil Action No. 07-357 (JJF) **CONSOLIDATED CASES**

AUO'S OPENING CLAIM CONSTRUCTION BRIEF

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'157 Patent	U.S. Patent No. 7,125,157
'160 Patent	U.S. Patent No. 6,778,160
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'781 Patent	U.S. Patent No. 6,976,781
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'984 Patent	U.S. Patent No. 6,803,984
AUO	AU Optronics Corporation and AU Optronics Corporation America
Chen Decl.	Declaration of Hua Chen in Support of AUO's Opening Claim Construction Brief
esp.	especially
Ex.	Exhibit
Fig.	Figure
Holloway Decl.	Declaration of Julie M. Holloway in Support of AUO's Opening Claim Construction Brief
JCC	Joint Claim Construction Chart [D.I. 376]
Joint Ex.	Joint Submission of Patents and Prosecution Histories (to be filed by the parties)
LGD	LG Display Co., Ltd. and LG Display America, Inc.

NOTES:

Emphasis added throughout, unless otherwise noted. In general, internal citations and quotations are omitted.

I. BACKGROUND OF THE TECHNOLOGY

The patents-at-issue relate to liquid crystal display (LCD) technology. An LCD device includes upper and lower substrates, such as plates of glass, with a liquid crystal material in between. Typically, the lower substrate has a matrix of thin film transistors ("TFTs") for controlling the amount of light emitted by each pixel in the display; the upper substrate has a matrix of color filters for controlling the color of each pixel. The LCD panel is then assembled with a backlight unit and other components to make a display module. AUO's patents relate to various aspects of LCD displays, such as the backlight unit and control circuitry. The majority of LGD's patents relate to the layout structure of the thin film transistor (TFT) or other specific configurations on the lower "TFT" substrate. Typically, an array matrix is formed with many crossing gate lines and data lines, with TFT located near each crossover point of the gate and data lines corresponding to a pixel electrode. The array matrix, along with the TFTs that control the pixel electrodes, is formed by laying/depositing, processing, and patterning different conductive, semi-conductive, and insulative material. This creates the layout structure for the TFT and other configurations on the active matrix array.

II. LEGAL STANDARD

"[W]e look to the words of the claims themselves, both asserted and nonasserted, to define the scope of the patented invention." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). Claim terms "are generally given their ordinary and customary meaning." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005). In some cases, the plain meaning may be readily apparent, in which case there may be no need to construe the terms. *Id.* at 1314; *see also U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (purpose of claim construction is to resolve disputes and "to ***clarify*** and when necessary to ***explain*** what the patentee covered by the claims"). Technical dictionaries and treatises can aid the Court in understanding the underlying technology and "the way in which one of skill in the art might use the claim terms." *Phillips*, 415 F.3d at 1318.

"[T]he claims themselves provide substantial guidance as to the meaning of particular

claim terms." *Phillips*, 415 F.3d at 1314. It is essential to consider the claim as whole when construing each term, because the context in which a term is used in a claim "can be highly instructive." *Id.* Furthermore, "the usage of a term in one claim can often illuminate the meaning of the same term in other claims." *Id.* at 1314.

A claim term can only be understood "with a full understanding of what the inventors actually invented and intended to envelop with the claim." *Id. at 1316.* Therefore, claim construction must begin with a full understanding of the invention as a whole. "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Id.* The specification is the primary basis for understanding the invention, and thus the claims. *Id.* at 1315. The specification "acts as a dictionary" both "when it expressly defines terms used in the claims" and "when it defines terms by implication." *Vitronics*, 90 F.3d at 1582. However, it is axiomatic that limitations from the specification may not be read into the claims. *See, e.g., Electro Med. Sys., S.A. v. Cooper Life Scis., Inc.,* 34 F.3d 1048, 1054 (Fed. Cir. 1994). "Where a specification does not ***require*** a limitation, that limitation should not be read from the specification into the claims." *Specialty Composites v. Cabot Corp.*, 845 F.2d 981, 987 (Fed. Cir. 1988) (emphasis in original).

III. AUO'S ASSERTED PATENTS

A. U.S. Patent No. 6,976,781, "Frame and Bezel Structure for Backlight Unit"

The '781 Patent is an important innovation in the assembly of the "backlight unit" for LCDs. A "backlight unit," as its name suggests, provides illumination from the back of the display. Backlight units are assembled between two frames: one on the viewing side of the display, and the other on the back side of the display. Typically, one frame is made of a flexible resin material while the other—referred to as a "bezel" in the '781 Patent—is made of a more rigid metal material. '781 Patent at 1:66-2:1; 2:13-16. In the prior art, designers of LCDs were forced to choose between an assembly with structural strength and one that was easy to disassemble. *Id.* at 2:20-22. The invention is new structure that offers both advantages. *Id.* at 2:29-32.

One prior art structure for assembling the backlight unit has the edges of the frame

mounted outside the sidewalls of the bezel, with outwardly-protruding hooks on the sidewalls of the bezel inserted into holes on the inner edges of the upper frame. *Id.* at 1:44-53, 1:64-66, Fig. 2. This structure is easy to disassemble but lacks structural strength. *Id.* at 2:4-7. A second prior art structure has the frame mounted inside the sidewalls of the bezel, with outwardly-protruding hooks on the edges of the frame inserted into holes on the inner sidewalls of the bezel. *Id.* at 1:54-63, Fig. 3. This second structure is relatively strong but difficult to disassemble, because the bezel, which is mounted outside the frame, is typically made of a rigid metal material. *Id.* at 2:8-20. The inventive assembly obtains both advantages by having (i) at least one sidewall of the rigid bezel outside the frame—for structural strength—and (ii) at least one edge of the flexible frame outside the bezel—for ease of disassembly. *Id.* at 2:33-50, 4:34-40.

While LGD has identified a number of longer terms of the '781 Patent for construction, six of these terms are simply larger terms including the disputed term "hooks." In reality, only the following four terms are disputed: hooks; bezel; "as said frame is mounted onto said bezel" and "simultaneously said second edge is disposed onto … second sidewall, and said first hooks are inserted and engaged in said second holes."

The parties dispute some aspects of the construction of "hooks." The parties agree that "hooks" are structures that protrude outwardly for the purpose of fastening a frame to a bezel. *Compare* AUO's construction ("any protruding structure intended to be inserted into a hole for the purpose of fastening one element to another"), *with* LGD's construction[1] ("protrusions … that extend outwardly from the first edge for fastening the frame to the bezel"). However, LG seeks to add a limitation to the term that is not supported by the intrinsic evidence. *See, e.g.*, *Vitronics*, 90 F.3d at 1582. Specifically, LGD's proposed construction requires that the "hooks" be "part of" the frame or bezel. It is immaterial to the invention whether the hooks are—or are not—part of the

[1] LGD incorrectly limits "hooks" to structures for fastening the frame to the ***bezel***. As in claim 6 and consistent with a proper construction of bezel (see discussion *infra*), hooks may likewise fasten a "lower frame" with an "upper frame."

frame, and the claims are not so limited. *See id.*

The parties dispute the meaning of the term "bezel." The plain meaning of "bezel" is a frame that typically is made of metal. *See, e.g.*, Holloway Decl., Ex. 9; *id.*, Ex. 10. LGD incorrectly contends that a "bezel" is limited to the "back cover" of the backlight unit. The specification and prosecution history make clear that a "bezel" may be either a front ***or*** back frame. If a bezel were only a "back cover," the '781 Patent would not refer to a "backbezel," as the modifier "back" would be wholly unnecessary and redundant. *See, e.g.*, *Broad. Innovation, LLC v. Echostar Commc'ns Corp.*, 240 F. Supp. 2d 1127, 1141-42 (D. Colo. 2003) ("displayable records" is a subset of "records" where both terms used in the specification); *see* '781 Patent at 1:30-33. Moreover, patents cited during prosecution—which are part of the intrinsic evidence—unmistakably depict bezels as front frames. *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003) (cited references are "intrinsic evidence"); *Phillips*, 415 F.3d at 1317; *see, e.g.*, Holloway Decl., Ex. 11 at 3:53-65, esp. 3:53-55, 3:59-60, and Fig. 1, item 40; Ex. 12 at 12:15-44, esp. 12:15-17 and Figs. 17 & 18, item 117.

The parties dispute the meaning of the terms "as said frame is mounted onto said bezel" and "simultaneously said second edge is disposed onto … second sidewall, and said first hooks are inserted and engaged in said second holes." Essentially, AUO's position is that these terms do not require the frame and bezel to be assembled simultaneously, and LGD's position is that they do. LGD's assertion that the mating of the hooks and holes of all the edges and sidewalls must occur at the exact "same time" finds no support in the specification or prosecution history. Rather, consistent with the plain meaning, these terms are used to describe the claimed ***structure***, which is assembled during a single process. In other words, the structure is ***configured*** such that a first plurality of hooks is mated with a first plurality of holes, and, at the same time, a second plurality of hooks is mated with a second plurality of holes. *See Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1324 (Fed. Cir. 2004) ("simultaneously merely requires a ***condition*** to exist at the same time or concurrently"). LGD's construction improperly seeks to read temporal limitations into apparatus claims. *See, e.g.*, *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1344

(Fed. Cir. 2008) ("Courts must generally take care to avoid reading process limitations into an apparatus claim … because the process by which a product is made is irrelevant to the question of whether that product infringes a pure apparatus claim…").

B. **U.S. Patent No. 7,101,069, "Direct Backlight Module"**

The '069 Patent discloses an improved backlight support. A backlight module includes one or more light sources, such as fluorescent lights; it also typically includes a reflecting plate, which serves to direct light to the viewing surface of the display, and a diffuser, which serves to uniformly distribute light from the light sources and reflecting plate across the viewing surface. In the prior art, as shown in Figures 1-2, there are separate supports provided for the illumination tubes (*e.g.*, fluorescent lamps) and to support the diffuser.

The improved backlight support ***simultaneously*** supports the diffuser and an illumination tube of an LCD module. *See, e.g.*, '069 Patent at 1:7-9, 1:44-46, 1:61-63, 2:39-41. As illustrated in Figures 3 and 4, the support includes two or more side walls that accommodate the illumination tube, and at least one of the side walls extends beyond the top of the illumination tube to support the diffuser. *See, e.g.*, *id.* at 3:34-42, 4:35-43, Figs. 3-4, 5A-5G. This structure prevents bending or deformation of the diffuser and illumination tube that can result from insufficient rigidity or thermal expansion and contraction. *See, e.g.*, *id.* at 1:46-52, 2:44-54.

The parties dispute the construction of the term "fitting portion." The '069 Patent teaches that the "fitting portion" is simply a structure for accommodating an illumination tube, as proposed by AUO. The plain language of the claims describes the fitting portion as a structure having two (*id.* at 4:35-40) or more (*id.* at 3:34-39) "side walls" into which an "illumination tube is disposed." The ordinary meaning of accommodate is "to fit" and the ordinary definition of "dispose" is "to place." Holloway Decl., Ex. 13 at 78-79; Ex. 14 at 820-1; Ex. 15 at 7, 330; Ex. 16 at 12, 654.

The specification confirms this as the proper construction, stating that the fitting portion is provided for "accommodating the illumination tube." '069 Patent at 2:62-64. The specification nowhere describes the fitting portion as "holding" an illumination tube, as required by LGD's construction. The fitting portion is consistently described only as a structure into which an

illumination tube "directly fits." *See, e.g.*, *id.* at Abstract, 1:57-65, 2:39-43. The figures depict a fitting portion having an opening into and from which an illumination tube may be freely moved. *Id.* at Figs. 5B, 5C, 5F, 5G. Figure 3 depicts a fitting portion having a ***gap*** between the side walls and the illumination tube. *Id.* at Fig. 3. This gap precludes the illumination tube from being "held."

The parties also dispute the proper construction of the claim terms "comprises two side walls extending upwardly and separately" and "has two side walls extending upwardly and separately." Notably, the only difference in language between these limitations, and claims 1 and 16 generally, are the terms "comprises" and "has" in claims 1 and 16, respectively. There is a presumption that these limitations have a different meaning, and indeed, the terms "comprises" and "has" do have different meanings. "Comprises" is a well-established, open-ended term meaning "having at least." Nothing in the intrinsic evidence contradicts this well-established meaning. Thus, this term is not limited to "includes," as proposed by LGD. The term "has," on the other hand, is simply the singular of have, a term with a widely-known plain and ordinary meaning. The proper construction of the terms "comprises" and "has" is "having at least" and "having," respectively. The remainder of the terms, "two side walls extending upwardly and separately" need not be construed. The term simply refers to two separate, generally ascending side walls. Figures 3, 4, and 5A-5G depict ascending side walls, portions of which are curved and portions of which are straight, confirming this plain and ordinary meaning. There is no basis in the intrinsic evidence to limit the side walls of claims 1 and 16 to "upright structures" as sought by LGD.

C. **U.S. Patent No. 7,125,157, "Backlight Unit"**

The invention of the '157 Patent allows a LCD to be rotated (*e.g.*, between portrait and landscape orientations) without causing defects in the optical film due to stress concentrations or expansion and contraction from temperature variation. '157 Patent at 5:46-54. These problems are common in the prior art where the optical film typically is securely fixed to the frame. *Id.* at 1:43-2:8. The '157 Patent solves these problems by having a frame with first and second protruding elements that alternate supporting the optical film depending upon the orientation of the LCD. For instance, when the LCD is in a first position (*e.g.*, portrait orientation) the first supporting portions

provide the sole support for the optical film. The second supporting portions, meanwhile, do not contact the second constraining portions on the optical film. *Id.* 2:12-26; 5:33-35. This arrangement prevents stress from building-up and allows for film expansion or contraction. *Id.* at 5:37-54.

While LGD identifies a number of longer terms to construe, the parties' actual dispute centers on six shorter terms, which are generally incorporated into these longer terms: "supporting portion;" "constraining portion;" "first position;" "second position;" "on opposite corners of the film;" and "on adjacent corners of the film."

The parties dispute some aspects of the term "supporting position." With the exception of LGD's construction of a "supporting portion" to mean a "projection," which improperly limits the claim language, the parties appear to be in agreement. The patent is clear in that it does not limit a supporting portion to any particular shape. *See id.* at 2:61-62 (each supporting portion "comprises a protrusion, a cylinder, or a cuboid"). However, a "projection," as recited in LGD's construction, may be defined to have a specific shape. *See, e.g.*, Holloway Decl., Ex. 17 ("Projection implies a jutting out esp[ecially] at a sharp angle."). Limiting the term "supporting portion" to "projection" also violates the doctrine of claim differentiation, since dependent claims 10 and 22 expressly recite a supporting portion that is "a protrusion, a cylinder, or a cuboid." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004). Indeed, LGD's proposed construction is ***narrower*** even than these dependent claims, which include not only protrusions but cylinders and cuboids. LGD's improper construction should be rejected.

The parties dispute the construction of "constraining portion." AUO's proposed construction, "any formation on or in the optical film (including but not limited to a hole or groove) intended to restrict the movement range of the film," is clearly supported by the specification. '157 Patent at 4:7-16 ("The holes are referred to as constraining portions as they constrain the movement range of the supporting portions."). The specification broadly defines a constraining portion to be a "hole or a groove" and to be "circular, elliptical, rectangular, rectangular with rounded corners, or polygonal." *Id.* at 2:27-30; 2:63-65.

LGD's proposed construction—"a passage through the film that has a gap in the gravity acting direction after receiving a supporting portion"—is incorrect and, because it is confusing, will not aid the jury in understanding the claims. *U.S. Surgical Corp.*, 103 F.3d at 1568 (purpose of claim construction is to resolve disputes and "to ***clarify*** and when necessary to ***explain*** what the patentee covered by the claims"). LGD improperly seeks to limit constraining portion to "a passage through the film" even though the specification expressly states that a constraining portion may be a "groove." *See, e.g.*, Holloway Decl., Ex.17 (defining "groove" as "a long narrow channel or depression"). LGD's construction also violates the doctrine of claim differentiation, improperly reading into "constraining portion" the limitation "gap"—which is present only in dependent claims 9 and 18.

The disputed term "first position," as defined in the specification, simply refers to an initial position of a LCD before it is rotated. *Id.* at 4:48-56 ("The first position is referred to as an initial position of the housing…"). Contrary to LGD's proposed construction, there is not any requirement that in a first position "the first projection is located near an upper edge of the frame." The claims describe the first position in terms of contact between the first and second supporting and constraining portions, not by reference to any specific location. *See id.* at 8:35-39, 10:12-16. LGD's construction is also improper because it (i) uses the unnecessarily narrow term "projection" (*see* discussion *supra*) and (ii) will not help the jury understand the claims.

AUO and LGD generally agree that the "second position" is a position determined by reference to the rotation between the first and second positions of the LCD. *Compare* AUO's construction ("the position is determined by reference to the angle of rotation between the first position and the second position"), *with* LGD's construction ("in an orientation rotated from the first position"). LGD's construction, however, is incorrect for the same reasons its construction of "first position" is incorrect.

The final disputed terms are "on opposite corners of the film" and "on adjacent corners of the film." These terms can be given their plain meaning. "Corner" is not a term of art, and no construction is necessary for the jury to understand this everyday term. LGD's constructions of the

terms "on opposite corners of the film" and "on adjacent corners of the film" needlessly injects confusion and ambiguity.[2] LGD's constructions are also improper because, as explained above, "constraining portions" are not limited to holes that are "through areas" of the film as LGD suggests. Rather, "constraining portions" may be holes or grooves that are "formed ***on***" the film, as recited in claims 6, 7, 20 and 21.

D. U.S. Patent No. 6,689,629, "Array Substrate for Display, Method of Manufacturing Array Substrate for Display and Display Device Using the Array Substrate"

The '629 Patent addresses a problem common in LCD manufacturing. Etching of the conductive patterns, *e.g.*, the wiring, on the array substrate is often uneven, because the etching rate will vary based on the wiring density: lower density typically results in faster etching. '629 Patent at 1:55-67. In areas where the wiring density is low—such as between the edge of the array and the connection pads at the edge of the substrate—the increased etching rate often results in "undercut" of the etched patterns. *Id.* at 1:61-67, 2:50-63. This can cause short-circuit defects in the display. *Id.* at 2:58-63. The invention of the '629 Patent solves these problems using the strategic placement of "dummy conductive patterns [] between the connection pads and pixel electrodes" of an LCD array substrate, in specified regions where the wiring density is low. *See, e.g.*, *id.* at 8:16-17. The dummy patterns, which preferably occupy 30% of these specified regions, increase the density of patterns to be etched in these regions, thereby enabling the formation of "good wiring over the entire surface of the array substrate ... without causing defects ... during etching [of] the scan lines [] and the signal lines" lying between the TFT array (and thus, the pixel electrodes) and the connection pads at the edge of the substrate. *Id.* at 5:33-38.

The parties dispute the construction of the term "area." As used in the '629 Patent, the term "area" refers to a specified region. This is consistent with the term's plain and ordinary

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[2] LGD's lengthy and ambiguous construction for the term "on opposite corners of the film" is "through areas where two edges of the film intersect such that the areas do not share an edge of the film." Similarly, LGD's construction for "on adjacent corners of the film" is "through areas where two edges of the film intersect such that the areas share one edge of the film."

meaning. Holloway Decl., Ex. 13 at 618-4. It is also consistent with the use of the term "area" in the claims: claims 1 and 9 use the term "area" to refer to a region of the array substrate, specifically the region where dummy conductive patterns are located. '629 Patent at 8:14-16, 8:58-60. The specification likewise defines the term "area" as the region where the dummy conductive patterns are formed. For example, the specification explains that, preferably, the substrate coverage "of the dummy conductive patterns themselves [is] 30% or more ***on an area of a specified surface***." *Id.* at 5:55-61; *see also id.* at 6:1-6, 6:38-40. LGD's position that the term "area" is indefinite is insupportable.

The parties dispute the construction of the term "a layer of an insulating substrate, having an area." The correct construction for this term is the claim language itself, given the construction of "area" discussed above. This plain meaning is consistent with the way the term is used in claim 9, which describes a method of forming, first, a layer of insulating substrate having an area, and then forming transistors and wiring ***on*** that layer of insulating substrate, followed by other components including dummy wiring on the area, *i.e.*, specified region, of the substrate. *See, e.g.*, *id.* at 8:45-63. This plain meaning is also consistent with how the term is used in the specification. *See, e.g.*, *id.* at 1:14-20, 3:12-20. LGD's proposed construction—"material deposited and patterned on a substrate, such as glass, that covers part of the array substrate surface" —bears no relation to the plain language of the claim and finds no support in the specification.

The parties dispute the construction of the term "a plurality of wiring arranged on the insulating substrate." Essentially, AUO's position is that this term refers to "two or more conductive paths," *i.e.*, wires, "disposed ***on*** the insulating substrate," while LGD's position appears to be that the "wiring" is in fact ***part of*** the layer of insulating substrate. AUO's proposed construction is simply a clarifying rewording of the plain language of the claims. AUO's construction is also entirely consistent with the descriptions in the specification, which repeatedly describes the formation of wiring, among other elements, ***on*** the insulating substrate. *Id.* at 1:14-20, 1:39-44, 2:13-19, 3:14-15, 3:33-34, 4:39-41, 6:1-6, 6:24-28; Figs. 1-4, 5(a)-(c), 11, 12(a)-(b). The intrinsic evidence nowhere describes a plurality of wiring that is ***part of*** the layer of insulating

substrate material, as required by LGD's proposed construct. Thus, LGD's position that the claimed "plurality of wiring arranged ***on*** the insulting substrate" be construed such that the plurality of wiring become "portions ***of*** the layer" is nonsensical and directly contradicts the plain language of the claims.

The parties dispute the construction of the term "each wiring." The plain meaning of "each wiring" is abundantly clear: it refers to the individual wires of the claimed "plurality of wiring." '629 Patent at 8:6, 8:11, 8:54-55. The claims plainly state that a first end of "each wiring" is in communication with at least one of the transistors of the thin film array. *Id.* at 8:7-9, 8:50-52. The specification further explains this connection of "each wiring," describing "wirings such as scan lines and signal lines connected with" the electrodes of the transistors. *Id.* at 1:17-19, 4:49-51, Fig. 2. LGD's position that "wiring" is indefinite is insupportable.

The parties dispute the construction of the term "dummy conductive patterns." In the context of the '629 Patent, the term "dummy conductive patterns" refers to one or more metal patterns that do not conduct signals or current used in the operation of the display. This meaning is confirmed, first, by the requirement in the claims "that the dummy patterns are not in contact with any of the wiring"—which wiring communicates with the transistors in the array. *Id.* at 8:13-19, 8:58-63. Moreover, this meaning is consistent with the specification which teaches that the dummy patterns are not needed for the operation of the circuit: they "are not in contact with any of the wiring" for the circuit (*id.* at 8:18-19), and "may be removed if necessary" (*id.* at 6:52-55) after the array substrate is manufactured.

LGD's proposed construct for "dummy conductive patterns" is incorrect. First, LGD's construct defines the dummy conductive patterns as "portions of the layer." The only layer in claims 1 and 9 is the insulating substrate layer. *Id.* at 8:2-19, 8:45-63. An ***insulating*** substrate cannot form "dummy ***conductive*** patterns." In addition, the specification teaches that the dummy conductive patterns can be formed of the same material and at the same time as the wiring—which wiring, according to the claims and the specification, is arranged ***on*** the insulating substrate. *See, e.g., id.* at 5:38-42. Nothing in the evidence requires "dummy conductive patterns" to be construed

such that they are unable to receive ***any*** voltages or signals.

The parties dispute the construction of the term "dummy conductive patterns comprising at least about 30% of the area of the insulating substrate, the dummy patterns situated between the connection pads and the pixel electrodes."[3] AUO contends that this term, properly construed, means dummy conductive patterns cover at least 30% of the region specified by where the dummy conductive patterns are formed; the dummy conductive patterns are situated between the connection pads and the pixel electrodes. According to the plain language of the claims, the dummy patterns must cover at least 30% of the area ***where the dummy patterns are situated***. *Id.* at 8:14-18, 8:58-61. That this is so is further explained in the specification.

Specifically, in one embodiment, the specification states that it is preferable that "the dummy conductive patterns [] ***themselves***" cover 30% or more of "an area of a specified surface." *Id.* at 5:55-58. In order for the dummy patterns ***themselves*** to cover 30% of this "area of a specified surface," the area of specified surface must be the "area of a specified region where the dummy conductive patterns are formed." *Id.* at 6:4-6. Further, as discussed above, the claims and the specification repeatedly and consistently describe the dummy patterns as "situated [on the insulating substrate] between the connection pads and the pixel electrodes." *See also id.* at 8:14-18, 8:58-61, Abstract, 3:17-18, 3:36-38, 5:29-33, 5:38-42, 5:47-49, 5:54-60, 5:62-65, 6:23-27, 6:31-34, Figures 2-4. No other location or limitations on the placement of dummy patterns are found in the intrinsic record.

The parties dispute the construction of the term "pixel electrode." A "pixel electrode" is an electrode for applying a driving voltage to a liquid crystal element in a liquid crystal display. The specification, referencing Figure 2, describes a "thin film transistor 21 that controls a potential of the pixel electrode." *Id.* at 4:48-49. The cited prior art—which is intrinsic evidence—notes that "pixel electrodes … function … for applying an electric field to the liquid crystals" or pixel of a

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[3] This term is in claim 1. Claim 9 includes a virtually identical term which should be construed in the same manner.

display. Holloway Decl., Ex. 20 at 1:61-64. Contrary to LGD's proposed construction, the cited prior art confirms that not all pixel electrodes are transparent. *Id.*, Ex. 21 at 8:37-39 (discussing both "pixel electrode[s]" and "transparent pixel electrode[s]").

E. U.S. Patent No. 6,778,160, "Liquid-Crystal Display, Liquid-Crystal Control Circuit, Flicker Inhibition Method, and Liquid Crystal Driving Method"

The '160 Patent discloses a method for "inhibiting flicker resulting from the poor response time of a liquid crystal display." '160 Patent at 1:11-12. This is achieved by applying an excess amount of pixel driving voltage to, or "overdriving," the liquid crystals ("LC") display elements of the display. *Id.* at 9:15-19. Through "overdriving the LC ..., the LC reaches [the target brightness level] in a short response time and the quantity of light [thereby] ... obtained ... is approximately the same as the quantity of light [] which would be provided [if the LC had] ... ideal response characteristic[s]," *i.e.*, if the LC was capable of instantaneously reaching a target brightness. *Id.* at 9:18-23. In other words, the liquid crystal is overdriven with a voltage that causes the crystal to output approximately the same quantity of light as would be provided by an "ideal" liquid crystal.

The parties dispute the meaning of the term "pixel." The plain and ordinary meaning of "pixel" is a picture element. *See, e.g.*, Holloway Decl., Ex 22 at 695-6, 698; Ex. 23 at 397; Ex. 24 at 466, 468; Ex. 25 at 527-8; Ex. 26 at 293; Ex. 27 at 655; Ex. 28 at 300; Ex. 17 at 897; Ex. 29 at 885 (each defining pixel as the small discrete elements that together form an image). The language of claim 4, for example, confirms this plain meaning, referring to "each of the pixels forming an image." '160 Patent at 11:51. The specification uses the term consistent with this plain meaning, for example referring to driving "each of the pixels forming an image." *Id.* at 3:40-42; *see also id.* at 1:43-45. In contrast, LGD's proposed construction, "an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change" improperly includes limitations that are nowhere supported by the intrinsic evidence.[4]

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[4] LGD's proposed construction for "frame buffer," which refers to "all pixels that form one complete picture," effectively admits that a pixel is an element of a picture or a "picture element."

The parties dispute the construction of the term "video signal." In the context of the '160 Patent, "video signal" simply refers to a signal comprising video information. This is the plain meaning of the term, and is consistent with its use in the specification. The '160 Patent explains, for example, that a video signal may be supplied by a personal or notebook computer ('160 Patent at 6:53-62), and that while the video signal may include "a plurality of color signals ... [including] R(read) [sic], G (green), B (blue) signals used in displays, other display systems can also be used." *Id.* at 5:6-14; *see also id.* at 11:45-46, 12:9-10, 14:3-8, Fig. 1. LGD's proposed construction, "a signal carrying a brightness level from a predetermined range," includes unnecessary limitations that are justified neither by the plain meaning nor by the intrinsic evidence. Moreover, LGD's construction will not aid the jury in understanding the claims: a lay person, familiar with television and video players, is capable of understanding what "video" means.

The parties dispute the meaning of the term "frame." According to the plain language of claim 12, a "frame buffer" provides storage for video information contained in a frame—the construction proposed by AUO. *Id.* at 13:3-4. Indeed, claim 12 expressly requires only that the frame buffer store "first brightness information for ***an*** input pixel," nothing more. *Id.* This minimum requirement is confirmed by the specification. *Id.* at 6:11-27. LGD's proposed construction, "a memory circuit or device that temporarily holds brightness levels for all pixels that form one complete picture on the liquid crystal display," includes unnecessary limitations, such as "all pixels" and "one complete picture." The specification describes a frame buffer capable of holding more data, but there is no reason to import this limitation into the claims.

The parties agree that the term "image displaying liquid crystal cell" is simply an image display element with a liquid crystal, as illustrated in Figure 1, item 32. Indeed, it is clear from the specification that a "liquid crystal cell [] outputs an image." *Id.* at 7:25-26. Further, the specification teaches "a driver for driving each of the ***pixels forming an image ... to a liquid crystal cell displaying the image***." *Id.* at 3:40-44. The parties dispute, however, whether the "image display element with a liquid crystal" should have an "ideal response characteristic at the maximum brightness change given the predetermined range of brightness levels." This portion of

LGD's proposed construction imports numerous limitations, such as "ideal response characteristic," "maximum brightness," and "predetermined range" that are justified neither by the plain meaning of the term nor by the intrinsic evidence.

The proper construction of the term "brightness level" is at the heart of a number of the parties' disputes.[5] The plain meaning of "brightness level" is "a level of intensity of light." Holloway Decl., Ex. 22 at 109; Ex. 30 at 550. This plain meaning is consistent with the specification which states brightness "should be considered in terms of the quantity of light" ('160 Patent at 8:32-35), *i.e.*, the intensity of light. LGD's proposed construction, "gray scale value or luminance value," improperly seeks to import limitations from the specification, and will not aid the jury in understanding the claims. While it is true that the specification indicates that a "brightness level can be ***represented*** as a target brightness value by a gray scale" (*id.* at 4:47-49), nowhere does the intrinsic record limit the representation of a video signal's brightness level to "gray scale values." With regard to "luminance value," according to the IEEE, "neither the term brightness, [nor] the term photometric brightness should be used to denote the concept of luminance" and vice versa. Holloway Decl., Ex. 22 at 546-1 (noting the imprecision of equating "brightness" with "luminance").

The correct construction of several disputed terms is straightforward, given the correct construction of "brightness level." The proper construction of the term "storage for storing the previous brightness level of the video signal input through said input logic" is memory that stores the previous level of intensity of light of the video signal input through the input logic. This is simply the plain meaning of the term. LGD's proposed construction, "memory that temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment," includes unnecessary limitations, such as "received from a host," that

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[5] These terms "storage for storing the previous brightness level of the video signal input through said input logic," "first brightness information for an input pixel," "second brightness information for the next input pixel," and "the next brightness level of the next video signal input to said input logic." The parties agree that "brightness information" refers to "brightness level."

are not justified by either the plain meaning of the term or the intrinsic evidence.

Similarly, the proper construction of "first brightness information for an input pixel" is simply the plain meaning, brightness level for an input pixel. LGD's proposed construction would be correct with the proper construction of "brightness level." The proper construction of "second brightness information for the next input pixel" is again the plain meaning, level of light intensity for a next input pixel. LGD's proposed construction, "the brightness level for the next frame of the input signal for the pixel," imports unnecessary limitations, such as "the next frame." Finally, the proper construction of "the next brightness level of the next video signal input to said input logic" is the brightness level for the pixel or sub-pixel (or video signal) during the next time increment input to said input logic. LGD's proposed construction, "the brightness level of the video signal received from the host input to the input logic for the next time increment," imports unnecessary limitations, such as "the host."

The parties dispute the construction of "determinator for determining an output brightness level" of claim 1. The parties appear to agree that this term refers to logic, such as circuitry, for determining an output brightness level. In fact, the claim expressly refers to the "determinator" as "said determination ***logic***," in the final element. '160 Patent at 11:34-35. However, LGD's proposed construction, "circuit or logic that determines the output brightness level *by applying an offset to the next brightness level that is predetermined based on a difference in quantity of light between the actual and ideal response characteristics of the liquid crystal cell*," improperly limits the claim by seeking to limit the *manner* in which the determinator determines the output brightness. There is no justification in the intrinsic evidence for the limitation LGD seeks to add.

The disputed term "substantially equal" means "a level that is not completely the same but can be accepted as a substantially equal level." This is simply the plain meaning of the term. The specification expressly defines the term, explaining that the "representation 'substantially equal level' refers to a level which is not completely the same but can be accepted as a substantially equivalent level." *Id.* at 4:56-58. This "substantially equal level" is further defined with reference to Figure 6 and the desire to obtain a "quantity of light (S") ... which is ***approximately the same as***

the quantity of light (S) ... [from an LC with] ideal response characteristic[s] (S".S)." *Id.* at 9:19-23; *see also id.* at 8:45-47 (quantity of light is "almost the same as" that of an ideal LC). LGD's proposed construction, "a level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than [sic] no preventive measures are taken," imports limitations from a preferred embodiment when there is no basis in the intrinsic record to so limit this term. Moreover, LGD's proposed construction contradicts the plain and ordinary meaning of "substantially equal."

The disputed term "time integration quantity of a brightness change" means "a quantity of light equal to the actual brightness level output through a liquid crystal, summed over the rise and fall response time of the liquid crystal." The plain meaning of integration, in this context, is summing a changing value (here, brightness level) over a period of time (here, the response time of the crystal). Holloway Decl., Ex. 31 (noun 1.a); Ex. 32 at 280-284, esp. 282, Definition of Definite Integral. The specification explains that "brightness of a pixel to the human eye … should be considered in terms of the quantity of light, that is, a brightness change integrated with respect to time." '160 Patent at 8:30-34. In other words, the change in the brightness level, integrated over a period of time, is a quantity of light. The specification confirms that the relevant period of time is the response time of the pixel, as illustrated in Figure 5. The specification includes examples for an ideal (stationary) and non-ideal (moving) response, Figures 4 and 5, respectively. For Figure 4, "the quantity of light (S) emitted in one time frame (T) is equal to L1xT (*i.e.*, brightness x time) as shown in the shaded area of Figure 4." *Id.* at 8:35-40; *see also id.* at 4:53-56. As shown in Figure 5A and 5B, where the image is moving and the response is thus non-ideal, the quantity of light S_A and S_B is the brightness integrated, *i.e.*, summed, over the rise and fall time of the response. *Id.* at 8:41-49. The term is thus not indefinite, as LGD asserts, but can be readily understood by a person of skill in the art.

The parties dispute the terms "ideal quantity of light in a stationary state" and "ideal light quantity which is the brightness in a stationary state." These terms refer to the quantity of light emitted by a pixel during one time increment when the pixel is in a non-changing, *i.e.*, stationary,

state. The specification teaches, by way of example, that an ideal quantity of light is that quantity of light output by an ideal LC over one time increment. *Id.* at 4:42-47, Fig. 4. An ideal LC does not exist (*id.* at 8:63-65); however, the specification's example teaches that the ideal quantity of light from a *conventional* LC is that quantity of light emitted from the LC during one time increment when the brightness is constant, *i.e.*, when the image is stationary. When the particular pixel or LC is driven at a target brightness for an entire time increment, the pixel or LC may be described as being in a non-changing or "stationary state." *Id.* at 8:37-39. LGD's proposed construction, "quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment," imports unnecessary limitations, such as "when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment" that are not supported by either the claim language or the specification, and will not aid the jury in understanding the claims.

The parties dispute the meaning of the term "offset." The plain and ordinary meaning of "offset" is a modification. This is confirmed by the plain language of claim 12 which requires an offset sufficient to make "the time integration quantity of a brightness change substantially equal to an ideal light quantity." *Id.* at 13:7-9. The specification describes, and thus implicitly defines, an offset as a modification to a pixel driving voltage. *Id.* at 2:4-12, 9:1-19, 9:40-63. LGD's proposed construction, "a value predetermined" imports unnecessary limitations, such as requiring that the value be "predetermined," that are not supported by either the claim language or the specification.

The parties dispute the construction of the term "an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information." This term simply refers to a modification to the second brightness information for making the time integration quantity of the brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state, with the terms "offset," "time integration quantity of a brightness change,"

"substantially equal," and "an ideal light quantity which is the brightness in a stationary state" construed as above. For at least the reasons stated in the discussion of the terms incorporated into this disputed term, LGD's proposed construction, "a value predetermined based on difference in quantity of light between the actual and ideal response characteristics of the pixel so that the quantity of light based on the actual response characteristic of the pixel to be substantially equal to the quantity of light based on the ideal response characteristic of the pixel when the pixel is provided with the second brightness level during the next frame and the first brightness level before and after the next frame," should be rejected.

Finally, the disputed term "so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to next brightness level" should be given its plain meaning, where the next brightness level is the brightness level that immediately follows the previous brightness level, and the terms "time integration quantity of a brightness change," "substantially equal" and "ideal quantity of light in a stationary state" are construed as above. For at least the reasons stated in the discussion of the terms incorporated into this disputed term, LGD's proposed construction, "so that the quantity of light based on the actual response characteristic of the liquid crystal cell is substantially equal to the quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment," should be rejected.

F. U.S. Patent No. 7,090,506, "Signal Transmission Device Having Flexible Printed Circuit Boards"

The '506 Patent teaches using "a signal transmission device communicating multiple signals between a liquid crystal display (LCD) module and a system." '506 Patent at 1:7-10. Specifically, the device joins two or more flexible printed circuit boards together, "connecting an LCD module and a system." *Id.* at 1:28. In contrast, the prior art requires two or more separate flexible printed circuit boards to achieve the same functionality, which incurs additional fabrication cost and space. *Id.* at 1:17-21. While LGD identifies a number of longer terms of the '506 Patent

to construe, the parties' actual dispute centers on four terms, which are generally incorporated into these longer terms.

The parties dispute the construction of "flexible printed circuit board," a common term in the art. The plain meaning of this term, as confirmed by several technical dictionaries, is "printed circuit made on a flexible film." For example, Microsoft's Computer Dictionary defines it as "[a] circuit printed on a thin sheet of flexible polymer film...." *See* Holloway Decl., Ex. 33 at 217. LGD's proposed construction, "flexible film with conductive patterns printed on its surface," (part of a longer term), is confusing and will not aid the jury.

The parties dispute the construction of the term "display module." The plain meaning of "display module," in the context of liquid crystal displays, is a liquid crystal display (LCD) module. The specification uses the term consistent with this plain meaning. *See, e.g.*, '506 Patent at 1:7-10 and 1:25-34. The prosecution history confirms this plain meaning. *See, e.g.*, Holloway Decl., Ex. 34 at 2-3; Ex. 35 at 2; Ex. 36 at 10. The cited references, which are intrinsic evidence, also clearly define "display module" as an LCD display. *See, e.g.*, Holloway Decl., Ex. 45 at 3:63-67 and 17:16-47; Ex. 37 at Abstract, 0003, 0008, 0018 and Fig. 1.

Nevertheless, LGD improperly seeks to import limitations from a specific embodiment in the specification to the claims, arguing that a display module necessarily includes a touch panel. It is axiomatic that limitations from the specification may not be read into the claims. *See, e.g.*, *Electro Med. Sys.*, 34 F.3d at 1054. It is well-established that "[g]eneral descriptive terms will ordinarily be given their full meaning; modifiers will not be added to broad terms standing alone." *Johnson Worldwide Assocs., Inc. v. Zebco Corp.*, 175 F.3d 985, 989 (Fed. Cir. 1999). The specification confirms that a "display module" does not require a touchscreen: when the inventors meant to refer to a touchscreen LCD module, they expressly described it as a "*touchscreen* display module," instead of the general descriptive term "display module." *Compare* '506 Patent at 1:65-67, 1:29-30.

The two disputed terms regarding the two bonding methods in the claims, "hot bar soldering" and "anisotropic conductive film (ACF) bonding," are also common terms with

definitive meanings in the art. Specifically, "hot bar soldering" describes a soldering process where the solder and flux are applied to the contact area and the contact area is heated with a bar to melt the solder. Holloway Decl., Ex. 38 at 29.49-55; Ex. 40 at 705-706. "Anisotropic conductive film (ACF) bonding" is to connect flexible circuit boards by a material that is substantially conductive in one direction after being pressed between the two circuit boards. Holloway Decl., Ex. 46 at 58; Ex. 39. LGD's proposed constructions are technically incorrect. Specifically, LGD's proposed construction for "hot bar soldering" is "a soldering process where the circuit boards are heated with a bar to melt the solder at multiple points simultaneously along each circuit board while pressure is applied to the connection." This construction is too narrow, as the only "pressure" necessary is to hold the two PCBs together during soldering, which is inherently part of the connection process. Holloway Decl., Ex. 38. at 29.49-55, Ex. 40, at 705-706. LGD's proposed to construe "anisotropic conductive film (ACF) bonding" as "a process where a material that is conductive in one direction is pressed between the two circuit boards." In fact, the material becomes conductive in one direction only after being pressed between the two circuit boards. LGD's construction is thus inaccurate and misleading. Holloway Decl., Ex. 39; Ex. 46 at 58.

G. U.S. Patent No. 5,748,266, "Color Filter, Liquid Crystal Display Panel, Liquid Crystal Display, and Liquid Crystal Display Panel Manufacturing Method"

The '266 Patent discloses a display panel consisting of two substrates: an array substrate, such as a sheet of glass, on which pixel electrodes are formed in rows and columns (*i.e.*, a matrix) and a color filter substrate, facing the array substrate, on which color filters are formed in a matrix. '266 Patent at 1:33-36, 2:7-12. The space between the substrates, sometimes called a "cell gap," should be "kept constant," otherwise "the display quality is deteriorated." *Id.* at 4:11-17. The invention "uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant." *Id.* at 4:65-67, Figure 8. In some cases, the pillars are covered with the common electrode to connect a storage capacitance line. By using this structure, "it is possible to supply the potential Vcom in which no signal delay occurs even around the central portion of a common electrode." *Id.* at 5:18-21.

The parties dispute the construction of "common electrode." In the context of the '266 Patent, this refers to a conductor, typically made of a transparent material, on the color filter substrate, which receives a reference voltage relative to which the pixel electrode voltages can be measured. LGD's construction turns the relationship between the reference voltage and the pixel electrode voltage upside down. While LGD's construction concedes that the common electrode receives a "reference voltage," it implies that this "reference voltage" is relative to the pixel electrode voltages. On the contrary, the purpose of the "reference voltage" is to be used as a reference for the pixel electrode voltages, not vice-versa. This is supported by the specification, which specifically discloses that in some cases, the common electrode potential can be constant. *See, e.g.*, *id.* at 2:61-66.

The parties dispute the construction of "storage capacitance line," and "storage capacitance line for outputting the reference potential of the storage capacitance." A storage capacitance line is simply a line or wire of conductive material, typically metal, connected to one or more storage capacitors of the TFT array. This is the plain meaning of the term, in the context of the '266 Patent. A "line," in the context of electronics, is a line or wire of conductive material, typically metal. Furthermore, as the claim language indicates, the storage capacitance line outputs the reference potential of the storage capacitance, and therefore is necessarily connected to one or more storage capacitors. *Id.* at 9:25-27. This plain meaning is consistent with the disclosures in the specification. For example, Figure 1 illustrates storage capacitors labeled 29, which are connected to storage capacitance line labeled 28. *Id.* at 1:45-48.

LGD's proposed construction— "a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors"—is defective in at least three ways. First, the substitution of "pattern of electrically conductive material" for "line" is overbroad and confusing, and does nothing to aid the jury in understanding the claims. Second, the line clearly does not "provide" a reference voltage—the plain language of the claims says the line is for "outputting" a reference potential. Third, there is no support in the claim language for the limitation "within the pixel area."

The parties have agreed upon constructions for "color filter," and "color filter substrate." Given these agreed-upon constructions, and constructions for "common electrode" and "storage capacitance line," discussed above, the following terms can be given their plain meaning: "objects formed on the array substrate"; "the pillars are covered with the common electrode"; "common electrode for all pixels covering at least some of the pillars"; "the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars." LGD's proffered construction for each of these terms is unnecessary, confusing and will not aid the jury in understanding what the claim means.

For example, LGD's proffered construction for "objects formed on the array substrate" is "structures having one or more patterned layers in the pixel array." Such a construction does not aid the jury in understanding the claims, and is unnecessary: a layperson understands what an "object" is. Similarly, for the two terms "pillars formed higher than the other portions of the color filter" and "pillars being formed higher than other portions of the facing substrate," LGD's proposed constructions are confusing and redundant. In addition, LGD's construction for "pillars formed higher than the other portions of the color filter" is technically incorrect on its face: the terms "color filter substrate" and "color filter" refer to distinct structures.

AUO's construction for "injecting liquid crystal between the array substrate and the color filter substrate"—"introducing liquid crystal into the space between the array substrate and the color filter substrate" – is its plain meaning to one of ordinary skill in the art and comports with its usage in the specification. The plain meaning of the word "inject" is "introduce." *See, e.g.*, Holloway Decl., Ex. 41 at 1164-3. The intrinsic evidence shows that injecting means introducing or filling, with or without injecting hole. *See, e.g.*, Holloway Decl., Ex. 42 at 2:15-18, 2:19-37, Fig. 2, 10:39-49, 11:15-22, 13:27-32 (liquid crystal is filled between the substrates without injection hole); *see also* Ex. 43 at 1:64-66 ("liquid crystal … is injected between the scribed substrates, which are then sealed."), Fig.1, 4:31-34 and Fig. 3. LGD improperly seeks to import the "injection hole" and "sealed" limitation of one specific embodiment—the "third embodiment"—into the claim. '266 Patent at 7:52. It is black letter law that "[w]here a

specification does not *require* a limitation, that limitation should not be read from the specification into the claims." *Specialty Composites*, 845 F.2d at 987 (emphasis in original); s*ee also Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998) ("limitations from the specification are not to be read into the claims").

As for the term "pillars of a color filter," the plain meaning of the term is pillars associated with or relating to the color filter. In the context, "of" means "relating to," as it is used in "judge of the case," or "belonging," as in "king of England." *See, e.g.*, Holloway Decl., Ex. 41 at 1565-11, Ex. 29 at 804-6.a. This plain meaning is consistent with the intrinsic evidence. The specification confirms that "color filter" and "pillar of a color filter" are associated, but distinct, structures that are formed separately. "In the first process, the color filter 32 is formed on the facing substrate 14, and the pillar 78 of a color filter is formed at a position corresponding to the hole 76 on the array substrate 12." '266 Patent at 8:20-23; *see also id.* at Figs 10 and 11, where the pillars are visibly delineated from the color filter.

LGD's proposed construction is "patterned structures that protrude toward the pixel array, to act as a spacer, and are made of color filter material." This proposed construction is defective in at least two ways. First, the term "pillar" is perfectly understandable to the jury, and there is no reason to substitute the confusing term "patterned structures that protrude toward the pixel array." Second, nothing in the claim language or the specification requires the pillars to be "made of color filter material." On the contrary, as discussed above, the specification confirms that the pillar is a distinct structure from the color filter.

H. U.S. Patent No. 6,734,944, Liquid Crystal Display

The '944 Patent also relates to improved spacers, and specifically to "spacers consisting of a photosensitive resin regulating the cell gaps" between two substrates of an LCD panel. '944 Patent at Abstract. "In the liquid crystal display of the present invention, characteristics and forms of spacers are set within a predetermined range." *Id.* at 2:51-54.

There are several terms in dispute, for each of which AUO has provided constructions, and each of which LGD asserts is indefinite. The specification of the patent provides detailed

descriptions of the terms in dispute, and the claims provide mathematical formulas, referring to known material characteristics and the desired ranges for those characteristics. The disputed claim terms thus could hardly be more definite: one of ordinary skill in the art can easily understand the "ordinary and accustomed meaning" of the claim terms based on the specification of the patent.

Specifically, the disputed term "at least one of the group consisting of" is standard language used for a Markush claim, which lists specified alternatives of a group in a patent claim. *See Abbott Labs. v. Baxter Pharm. Prods., Inc.*, 334 F.3d 1274, 1281 (Fed. Cir. 2003) (specifically pointed out that "at least one member of the group" as qualifying language of a Markush claim).[6] "Elastic coefficient" is a value that defines the elasticity of a material, which was readily understood by the examiner and the inventors through the prosecution process. *See, e.g.*, Holloway Decl., Ex. 44 at 5. The term "Dynamic Hardness value DH" is defined as: $DH=K\times P\text{max}/h\text{max}^2$. Constant K is defined by the specification as "a value obtained by the variation of an indentation inherent to the liquid crystal display". '944 Patent at 3:66-4:1. As a further illustration, an example is shown in the specification to obtain these values. *Id.* at 7:27-30. "Hardness value of plastic deformation (HV)" is also defined in correlation to the term DH. Finally, the term "the length of one side of the upper spacer surface" defines the length of one side of the upper spacer surface which can be measured by the method taught in detail in the patent (*See id.* at 5:49-6:14, and Figs. 2A and 2B).

IV. LGD'S ASSERTED PATENTS

For the Court's convenience, a chart summarizing the asserted claims, the disputed terms, the parties' proposed constructions, and any prior constructions of the terms by a court is attached to the brief as Appendix A.

A. Common Terms

AUO submits that the "transistor/TFT", "gate electrode/gate", and "XXX formed on YYY"

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[6] Despite its claim of indefiniteness, LGD proffered a construction for this term identical to AUO's.

terms found in the '737, '449, '002, '569, '274, '321, and/or '489 Patents should be construed uniformly across the patents. None of these patents utilize the terms in any specialized manner, and nothing in the patents suggests any meaning other than their plain meaning to one skilled in the art. These terms should therefore be construed uniformly, according to their plain meaning.

LGD proposes a number of different constructions for each of these standard terms, suggesting that their meaning differs between some of the patents, while maintaining that they have the same meaning among others.[7] The specifications of the patents do not use the terms in any differing or particularized way, so AUO contends that LGD's attempt to construe the terms differently for different patents is an improper attempt to redefine the terms.

1. **"thin-film transistor" ('737 Patent) / "thin film transistor" ('449 Patent) / "transistor" ('274, '321, '489 Patents)**

AUO proposes that these terms be construed uniformly as "a three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer." This construction captures the plain meaning of the term to one of ordinary skill in the art and is consistent with the specification of each of the patents in which it appears.

LGD's proposed constructions contain differ from each other and from AUO's proposed uniform construction. LGD's proposed construction for "thin-film transistor" as used in the '737 Patent differs from AUO's proposed construction only as to the use of the word "electrode." Rather than identifying the three terminals of the semiconductor device as "electrodes," LGD chooses to refer to them as "terminals." LGD's proposed construction for "thin film transistor" as

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[7] For example, LGD proposes that "transistor" as used in the '274 Patent be construed differently from "transistor" as used in the '321 and '489 Patents, even though the three patents have identical disclosures. Not surprisingly, LGD identifies no support in the specification as to why (continued...)

used in the '449 Patent specifies that a thin film transistor is "a three terminal device" rather than a "three terminal semiconductor device." And for the '274 Patent, LGD proposes that "the thin film transistor is formed using thin-film techniques on a substrate" rather than "using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer," as it proposes for the rest of the relevant patents. These differences are not supported by the intrinsic evidence.

a. **The "thin film transistor" of the '449 Patent is a semiconductor device.**

LGD's construction suggests that the thin film transistor disclosed in the '449 Patent is not a semiconductor device, or at least seeks to broaden the scope of the term's meaning beyond that supported by the disclosure.

The '449 Patent discloses a thin film transistor device that contains conducting, semiconducting, and insulating films layered on top of each other. The structural description of the invention, consistent with AUO's proposed construction, includes "a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; [and] a source electrode and a drain electrode formed on the semiconductor layer." '449 Patent at 2:42-45. Moreover, "[t]o further accomplish the objective of the present invention" (*id.* at 2:56-57) the '449 Patent discloses the method of manufacturing using conductive, insulating and semiconducting films. *Id.* at 2:57-65.[8]

Thus, the specification of the '449 Patent provides no support for construing the term "thin film transistor" any differently from the way it should be construed in the other patents, or giving it any meaning other than its plain meaning to one of ordinary skill in the art.

(...continued from previous page)
this term should be construed differently in the '274 Patent.

[8] *See also* '274 Patent at 4:63-5:3. This disclosure corresponds exactly to "sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; [and] patterning the impurity-doped semiconductor layer and semiconductor and layer to an active pattern." '449 Patent at 2:61-65. *Compare also* '449 Patent, Fig. 2 *with* '274 Patent, Fig. 4.

b. **The "transistor" of the '274 Patent is formed on an insulating substrate, and not on a single crystal silicon wafer.**

LGD provides no reason why the term "transistor" as used in the '274 Patent should be construed differently from "transistor" as used in the '321 and '489 Patents, given that the three patents have identical disclosures. LGD seems to acknowledge that the term as used in the '321 and '489 Patents should be construed consistently with "thin-film transistor" as used in the '737 Patent and "thin film transistor" as used in the '449 Patent. Those two patents confirm that the substrate is insulating. *See, e.g.*, '737 Patent at 2:10-14l; '449 Patent at 3:43-45.

2. **"gate electrode" ('737, '449, '569 Patents) / "gate" ('274, '321, '489 Patents)**

AUO proposes that these terms be construed uniformly as "a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode." AUO believes that this construction provides the most consistent understanding of the types of electrodes used by the inventions of the patents.

Another court previously construed "gate electrode" in the '737 Patent to mean "a patterned, electrically conductive material that controls current flow through the channel between the source electrode and the drain electrode," and "source electrode"[9] to mean "a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode." AUO's proposed construction for "gate electrode" seeks to conform the construction to the prior court construction for "source electrode" and "drain electrode." AUO believes that construing the "gate electrode" to be formed in the gate region serves to clarify the prior construction.

a. **"Gate electrode" and "gate" are used interchangeably and should be construed uniformly.**

The patents demonstrate that "gate electrode" and "gate" refer to the same structure. The

[9] "Drain electrode" was construed in an identical manner, other than identifying it as being formed over the "drain region."

'737 Patent states that the initial step in fabricating its thin film transistor is "forming a gate electrode 2 on an insulating substrate 1." '737 Patent at 2:11-12. In the '449 Patent, "a conductive layer is formed on a transparent glass substrate 1 and patterned to form a gate electrode 2." '449 Patent at 3:43-45. And in the '569 Patent, "a first metal layer is formed on substrate 111 … [and] patterned so as to form the gate line 113" and "a portion of the gate line 113 is etched so as to form the inverted 'T'-shaped opening 114 and the gate electrode 115 is defined there around." '569 Patent at 6:21-31. In the '274, '321, and '489 Patents, "[t]he gate 49 has a double-layered structure including the first and second metal layers 43 and 45 disposed on the substrate 41." '274 Patent at 4:32-34.

b. **LGD also provides interchangeable constructions for "gate electrode" and "gate".**

Furthermore, LGD provides identical constructions for "gate electrode" as used in the '569 Patent and "gate" as used in the '274, '321, and '489 Patents, proposing that the term as it is used in each of these four patents should be construed to mean "patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode." This definition only differs from LGD's proposed construction for "gate electrode" as used in the '737 and '449 Patents in that it includes the phrase "that includes a portion." LGD cannot adequately explain why that phrase should be added for certain patents, and AUO proposes it should be omitted from the construction entirely.

3. **"XXX formed on YYY" ('449 Patent, claim 1) or "forming XXX on YYY…" ('321 Patent, claims 7 and 16;'737 Patent, claim 1;'002 Patent, claim 1)**

Another common term that is used in several patents is "forming/formed on": either "XXX formed on YYY" or "forming XXX on YYY". The parties have chosen seven instances of this term (one in each of the '737, '002 and '321 Patents, and four times in the '449 Patent) for construction. In each instance "forming/formed on", ***as used in those seven limitations***, means "…above, supported by, ***and*** in contact with…" The Court should adopt AUO's proposed construction to make this clear.

AUO's construction is consistent with how the term "forming/formed on" is used within

the respective claim limitations, recognizing that a claim term is to be read "in the context of the particular claim in which the disputed term appears." *See Phillips*, 415 F.3d at 1313. While LGD agrees that the five instances in the claims of the '449 and '321 Patents require "above and in contact" (*see* JCC, Ex. C, pp. 2-5 and Ex. G, p. 2), LGD changes its position for the two instances in the '737 and '002 Patents and asks the Court for a construction of "above and supported by or in contact with". *See* JCC, Ex. A, p. 3 and Ex. B, p. 1. This shift in position by LGD is illogical, as the claim term "forming…on" is specifically used in the claim limitations at issue—i.e., '737 patent, Claim 1 ("forming a gate electrode on an insulating substrate"); '002 Patent, Claim 1 ("forming a pattern of pixels on said substrate")—to denote forming one layer/pattern above and in contact with the layer/pattern below it. *Id.* In the '737 patent, the gate electrode 2 is formed above and in contact with the insulating substrate 1 that sits directly below it. *See* '737 Patent at Figs. 2-3, 2:8-16, 3:23-28. Similarly, in the '002 Patent, the pixel pattern is also formed above and in contact with the substrate. *See* '002 Patent at 5:24-32; 5:2-6; *see also* Figs. 3 (ITO 46 on the left in the area of pixel pad 68) and 6 (pixel 166). The surrounding claim language of Claim 1 of the '737 and '002 Patents also dictates such reading. *See* '737 Patent at 4:25-46; '002 Patent at 8:65-9:12. Thus, the Court should reject LGD's disregard of the claim language and the intrinsic evidence, and adopt AUO's proposed construction.

B. **U.S. Patent No. 4,624,737, "Process for Producing Thin-Film Transistor"**

The '737 Patent relates to a process for manufacturing a thin-film transistor; in particular, a bottom-gate staggered amorphous-silicon (a-Si) structure. *See* '737 Patent at Figs. 2e and 3d. As Fig. 2e illustrates, this bottom-gate staggered amorphous-silicon (a-Si) structure is comprised of multiple thin-film layers. For bottom to top, these layers are: a gate (2); a gate insulating layer (3); an amorphous silicon layer (4); an n+ amorphous silicon layer (25, 26); a source and drain electrode layer (15, 16); and a passivation layer (8). Only Claim 1 of the '737 Patent is at issue.

1. **"continuously depositing" (claim 1)**

AUO proposes that this limitation be construed as "precipitating… without intervening films." The difference between AUO and LGD's proposal lies in what the verb "deposit" means.

According to LGD's proposal, the term "depositing" means "the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film."

AUO's construction is consistent with both the specification of the patent and the plain meaning of the term. To start, the dictionary meaning of "deposit" is "to lay or throw down by a natural process; precipitate." Chen Decl., Ex. 1, THE RANDOM HOUSE DICTIONARY OF THE ENGLISH LANGUAGE 535 (2nd ed. 1987). The deposition process disclosed in the '737 Patent also requires a precipitating process. As an example, the specification teaches one way to form a gate insulating film is to have a mixed gas of SiH4 and NH3 injected in a chamber, and let the gas precipitate to form a thin-film layer. *See* '737 Patent at 2:23-30. LGD's proposal, on the other hand, is impermissibly broad because it ignores the choice of the word "deposit" and allows ***any*** formation process.

2. **"without exposing them to an oxidizing atmosphere"/ "oxidizing atmosphere" (claim 1)**

These limitations should be construed respectively as "without exposing them[10] to an atmosphere containing an oxidizing agent," and "atmosphere containing an oxidizing agent." AUO's proposal reflects the plain meaning of the claim language, and it is further supported by the specification of the patent.

The '737 Patent, for example, states that a gate insulating film, a high-resistivity film, a low-resistivity film, and a conducting film are successively formed "without exposing them to an oxidizing atmosphere." '737 Patent at 2:18-24. The disclosed process is said to be advantageous over the prior art because no oxides are formed over the interfacing regions as a result, and good junctions from one thin-film layer to another can be achieved. *Compare id.* at 3:33-59 *with id.* at 1:32-46. LGD's proposed construction, on the other hand, directly contradicts the specification. *See id.* at Abstract ("A gate insulating film, a high-resistivity semiconductor film, … are successively deposited in lamination without exposing them to ***any*** oxidizing atmosphere including

[10] AUO's position is that the term "them" is indefinite. *See* JCC, Ex. A.

atmospheric air.") (emphasis added).[11]

3. **"a fourth step for selectively forming a source electrode and a drain electrode" (claim 1)**

This limitation should be construed as a step-plus-function limitation under Section 112, paragraph 6. 35 U.S.C. § 112. The function of this limitation is "selectively forming a source and drain electrode," and the corresponding acts are disclosed in Figures 2d and 3c, and at 2:60-62 and 3:37-41.

It is well established case law that the use of the "step for" phrase in a method or process claim invokes the presumption that Section 112, paragraph 6 applies. *Masco Corp. v. U.S.*, 303 F.3d 1316, 1327-28 (Fed. Cir. 2002); *Greenberg v. Ethicon Endo-Surgery, Inc.*, 91 F.3d 1580, 1583 (Fed. Cir. 1996) ("[I]n the context of method claims, the use of the term 'steps for' signals the drafter's intent to invoke Section 112, paragraph 6."). LGD cannot overcome the presumption because the claim language is better characterized as describing "what [the claimed] element ultimately accomplishes in relationship to what the other elements of the claim and the claim as a whole accomplish," rather than describing "how the function is accomplished." *See Seal-Flex, Inc. v. Athletic Track and Court Construction*, 172 F.3d 836, 849-50 (Fed. Cir. 1999) (J. Rader concurring) (noting that the former corresponds to "function" and the latter corresponds to "acts").

4. **"said source and drain electrodes serving as at least a part of the mask" (claim 1)**

AUO contends that this limitation should be construed as "using the source and drain electrodes to partially define the boundary for the removal or formation of the conductive film."

The parties dispute how the source and drain electrodes play a "mask" role. AUO's

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[11] LGD's proposal also lacks any support from the intrinsic evidence. Neither the claim language specifies the amount of oxidizing agent (or level of oxidization on a film) that is or is not allowed in the claimed process, nor does the specification or file history provide a quantitative measure as to what is detectable or not, or at a minimum provide a technique to measure the amount of oxidization of a film. LGD's proposal would further create a validity issue because the construction is indefinite as to scope; the phrase "detectable amount" does not identify the scope of what is claimed.

proposal emphasizes that the source and drain electrode is part of mask because it defines the boundary for removal; LGD's proposal emphasizes only the physical properties of the materials by proposing that the electrodes are part of a pattern that is more resistive to removal technique than the material to be removed. JCC, Ex. A.

AUO's emphasis better reflects the teachings of the '737 Patent. As evident from Figs. 2c and 2d of the '737 Patent, the source and drain electrode members (elements 15 and 16) shield the portions of the conductive film 30 and the low-resistivity amorphous silicon film 20 underneath them. *See* '737 Patent at 2:54-66. In other words, the source and drain electrode serve "as at least a part of the mask" by partly defining the boundary of removal – the material enclosed by the edges between the source and drain electrodes is to be removed.

AUO's construction is also consistent with the claims requirement of two distinct steps: a fourth step for selectively forming a source electrode and a drain electrode; and a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask. Based on the claim language, after the drain and source electrodes are formed, the two electrodes are used at least a part of the mask to selectively remove the conducting film. While it is unclear how the electrodes are used as "a part" of the mask, it is obvious based on the claim language that the drain and source electrodes are used to define the boundary of where to remove the conducting film exposed on the island region.

Because LGD's construction only focuses on the physical properties of the materials, LGD's construction fails to acknowledge the boundary-defining role by the source and drain electrodes. While LGD's lengthy construction indicates that the source and drain electrodes are a part of a "pattern" involved in selectively removing material from a surface underneath this pattern, it does not indicate how the pattern is related to the selective removal.

C. U.S. Patent No. 5,019,002, "Method of Manufacturing Flat Panel Backplanes Including Electrostatic Discharge Prevention and Displays Made Thereby"

The '002 Patent teaches a specific circuitry design for providing electrostatic discharge (ESD) protection during the manufacture of an active matrix display device such as an LCD

display, and further claims a method that employs such a design during manufacturing. Specifically, the patent discloses a process that utilizes ring structures surrounding the active elements of a display to guard against ESD, thus providing protection.

This Court has previously construed a number of terms and phrases of Claims 1 and 8 of the '002 Patent in a prior case, *LG. Philips LCD Co., Ltd.* (currently LG Display) *v. Tatung Company et al.*, No. 05-292 (JJF) (the "CPT case"). AUO's claim construction proposals are consistent with and, at times, further clarify[12] this Court's prior constructions in that case.[13]

1. **"forming a plurality of row and column intersecting pixel activation lines" (claim 1)**

This limitation should be construed as "forming a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines." JCC, Ex. B, p. 2. This proposal flows directly from the ordinary meaning of the claim language, and makes clear that sets of both a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines are formed. Such sets of intersecting pixel activation lines are further supported by the specification. *See, e.g.*, '002 Patent at Figs. 1, 4-6; 3:25-57; 4:53-58; 5:58-6:17. In contrast, LGD's construction fails to clearly recognize the distinction and further reads

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[12] In numerous instances, AUO asks the Court to construe the claim limitations as a complete phrase, instead of discrete claim terms. To the extent that the Court previously construed elements within a single phrase but not the entire phrase, AUO believes that a construction of the phrase as a whole will clarify the meaning of the limitation. Finally, and with respect to certain discrete claim terms that this Court previously construed, AUO believes that the prior constructions from the CPT case may be open to differing interpretations, and respectfully contends that further clarification of a few previous constructions as part of the process of construing the overall phrase to which those terms belong may prevent unnecessary future disputes and avoid changing the scope of the claims in a way the Court may not have intended by its construction in the CPT case.

[13] As the Federal Circuit recently pointed out in *O2 Micro International, Ltd. v. Beyond Innovation Technology Co., Ltd.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008), the purpose of claim construction is not just to define specific terms, but also to define the proper scope of the claim. Construing the entire phrase also preserves the relationships within and between the limitations. *Phillips*, 415 F.3d at 1314 ("[T]he context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms.")

away limitations such as "a plurality of," "intersecting," and "activation lines." Thus, AUO's proposed construction is the proper one.

2. **"interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another" and "interconnecting" and "substantially all" (claim 1)**

The main dispute here between the parties appears to rest on the portion interconnecting "substantially all of said XXX lines to one another," which AUO submits should mean joining "almost all of the XXX lines together." LGD argues that it means connecting "all or nearly all XXX lines to at least one other XXX line," but this proposal introduces ambiguity and is faulty for several reasons. LGD illogically seeks to redefine "to one another" as "to at least one other row/column line." LGD's proposal is unnecessary and has no support in the specification. AUO's proposal is entirely consistent with the patent's teaching on joining the row lines together as well as joining the column lines together. *See, e.g.*, '002 Patent at 8:5-8 ("interconnecting" through joining the row (or column) lines by "serially connect[ing] together via jumpers"); *see also* Chen Decl., Ex. 2, U.S. Patent No. 4,820,222 (the "'222 Patent")[14] at 6:51-55, 6:61-65, 7:39-55.

AUO further believes that the word "joining" here would better serve to clarify the meaning of "interconnecting," which was previously construed by this Court to mean "electrically connecting with conductors." As this Court previously recognized, "'[i]nterconnecting' is consistently described or illustrated in figures as using 'lines', 'shorts', or 'jumpers', i.e., conductors, to connect electrical elements," with a set of jumpers/lines/shorts being used to join the row lines together and another set of jumpers/lines/shorts being used to join the column lines together. Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 6; *see, e.g.*, '002 Patent at 8:5-8; *see also e.g.*, Chen Decl., Ex. 2, '222 patent, Figs. 6 and 7; 6:51-55; 6:61-65; 7:39-55. However, the previous construction of "electrically connecting" is not very clear as it denotes the possibility of indirect connecting and may lead to ambiguity and inconsistency with the clear

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[14] As this Court has already recognized, the '222 Patent has the same inventor as the '002 patent and is incorporated by reference in the '002 patent. *See* '002 Patent at 2:30-36; *see also* Chen (continued...)

teaching of the patent that the row lines be joined together and the column lines be joined together.

Consistent with the plain meaning and the teaching of the patent, the entire limitation, including the two sub-parts, should be construed as "joining almost all of the row lines together and joining almost all of the column lines together."

3. **"outer electrostatic discharge guard ring" (claim 1)**

AUO contends that this limitation should be construed as "a surrounding structure outside the active matrix display to provide protection from electrostatic discharges." JCC, Ex. B, p. 7. The only dispute between the parties is whether the outer guard ring should be construed as "a closed or open ring, or open L or C-shaped line" (LGD's position) or "a surrounding structure" (AUO's position). *Id.* AUO notes that this Court previously adopted the former construction based upon the agreement of both CPT and LGD that the outer guard ring is "a closed or open ring, or open L or C-shaped ring." Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 8 ("CPT does not dispute that the outer guard ring is 'a closed or open ring, or open L or C-shaped line.'"). However, this previously agreed construction, proposed now again by LGD, defies plain meaning, and a close reading of the specification reveals its errors.

The plain meaning of "ring" is "a circular or surrounding line or mark,"[15] which is consistent with AUO's proposed construction of "a surrounding structure." While the specification describes the internal (or inner) ESD guard ring 114 is "a closed ring, but could also be an open L or C-shaped line" ('002 Patent at 7:18-21), such description was never used to describe the outer ESD guard ring 200.[16] In fact, this suggests that the term "ring" would not otherwise include an L

(...continued from previous page)
Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 6 fn.1.

[15] Chen Decl., Ex. 1, THE RANDOM HOUSE DICTIONARY OF THE ENGLISH LANGUAGE 1658 (2nd Ed. 1987).

[16] There is no dispute that the '002 patent describes two distinct type ESD rings: a permanent internal guard ring that remains after manufacturing process is completed, and a removable outer guard ring that is removed at the end of the manufacturing process.

or C-shaped line.[17] Moreover, the specification and drawing consistently describe the outer ESD guard ring as a surrounding structure, illustrating in Fig. 7, just "one corner portion of…the outer guard ring 200" with the "corner pad 208 [connecting] to each other corner pad (not illustrated) by respective outer conductive lines 210 and 212 of the [outer] guard ring 200." *See id.* at 8:3-4, 8:8-11. With each of the four corner pads connected by the "respective outer conductive lines 210 and 212 of the [outer] guard ring 200," the surrounding structure of the outer ESD guard ring is formed. *Id.* As such, AUO's construction is proper, and the Court should adopt it.

4. **"resistance" (claim 1)**

AUO contends that this limitation, which represents the circuit component that couples the outer ESD guard ring to the interconnected row and column lines, should be construed as "a circuit component that has a specified ratio between voltage and the flow of electric current, and used to minimize the current surge from electrostatic discharge." AUO's proposed construction parallels closely with the construction set forth previously by this Court. *See* Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 13. However, rather than using the word "resistance" (as part of "resistance to the flow of electric current") again in the construction for the term "resistance," AUO respectfully submits that better clarity will result by further defining "resistance to the flow of electric current" in the Court's prior construction. AUO's proposed construction with the certain specified ratio further comports with the technical definition for "resistance."[18]

As the Court correctly noted, "the only guidance for construction here is how 'resistance' is

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[17] Importantly, the specification even makes clear when the internal/inner ESD guard ring 114 would retain an open L or C-shaped line as opposed to a closed ring shape: "…be an open L or C-shaped line ***if*** the gate and source pads all are on one respective side of the display (*emphasis added*)." *See* '002 Patent at 7:19-21. Because the outer ESD guard ring is outside of the active matrix display under the parties' proposed construction, it is necessarily outside the gate and source pads that potentially affect the shape of the internal/inner EDS guard ring.

[18] *See* Chen Decl., Ex. 4, IEEE STANDARD DICTIONARY OF ELECTRICAL AND ELECTRONICS TERMS 828 (4th Ed. 1988) ("resistance" in the context of the '002 patent is a specified value represented by "the quotient [i.e., ratio] of the voltage developed across the instrument terminals to the current passing between the current terminals.")

used in the single embodiment in which it appears" because of the "coextensive[ness]". *Id.* at p. 12. Here, this "resistance" is not just any resistance, but "a large resistance 228, such as 100 K ohms (illustrated schematically)". *See* '002 Patent at 8:25-26. As the Court also noted, the large resistance 228 is described in the following context: "...connected to the other set of gate or source lines by a shunt line 224, a shunt transistor 226 and a large resistance 228." By using the terms "line," "transistor," and "resistance" together for different components, the specification tells a personal of ordinary skill in the art that one is not the same as the other.[19]

In contrast, LGD's proposal of "a circuit component designed to provide opposition to electric current flowing through itself..." contradicts the intrinsic evidence and conflicts with this Court's previous ruling. In particular, LGD seeks to read away the "specified" value of resistance dictated by the specification and specifically noted and incorporated by this Court into the prior construction. *See* Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, pp. 12-13. By neglecting the clear teaching of "specified" resistance, and in fact, a large specified resistance, to "provide protection from [ESD] between the row and column activation lines during manufacturing," LGD ignores the teaching of the patent and further disregards this Court's prior analysis dictating that one is to look for guidance within the single embodiment shown in Fig. 7. *See* '002 Patent at 8:1-39. The Court should, therefore, reject LGD's proposed construction in favor of AUO's clear construction.

5. **"to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the display" and "protection from electrostatic discharges" and "row and column activation lines" (claim 1)**

AUO contends that this whole limitation, including two sub-parts, should be construed as "to guard against electrostatic discharges between the row activation lines and column activation lines during the manufacturing of the displays." AUO's construction is more consistent with the

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[19] As this Court also correctly indicated, "the patentee explicitly stated that certain elements of the invention could vary from the specific descriptions in that embodiment, but did not include the 'resistance' among those elements. ('002 Patent at 8, ll. 49-62.)."

plain meaning[20] of this limitation than LGD's proposal of "to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display."

The term "provide protection from electrostatic discharge..." is consistently used in the specification to mean "to guard against electrostatic discharges," providing "protection against fatal defects during and after manufacture of the displays." *See* '002 Patent at 2:40-42; *see also id.* at 8:1-2, 8:30-31 (providing "an ESD short…"); 3:54-68. "Minimizing" current surge simply does not capture the full scope of the ESD protection disclosed in the '002 Patent.

With respect to the second subpart, LGD's proposal completely misses the mark. In fact, LGD's proposal completely ignores the language "between said row and column lines". The specification makes clear that the ESD guard rings are "provided to protect the active elements of the display from the potential discharge between the row and column lines." *See id.* at Abstract; *see also id.* at 2:57-62; 8:1-39. LGD's proposed construction is improper and should be rejected.

6. **"removing said outer guard ring and row and column interconnections" and "removing" (claim 1)**

AUO contends that the entire limitation, with one sub-part "removing," is indefinite, but in the event that the Court construes it, it should be construed as "physically disconnecting (removal of) said guard ring and lines connecting/joining the row and column, intersecting pixel activation lines from the substrate." This proposed construction is consistent with this Court's prior construction and recognition that "removing" refers to the "removal of the guard ring and row and column interconnections from the display panel" in the specification. Chen Decl., Ex. 3, Judge Farnan Memorandum Opinion, p. 7. As this Court puts it, "the intrinsic evidence indicates that physical removal of the outer guard ring is precisely what the patent teaches." *Id.* at p. 9.

The only clarification that AUO seeks is for this Court to specify is that the "row and column interconnections" to be removed are "lines connecting/joining the row and column

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[20] *See* Chen Decl., Ex. 1, THE RANDOM HOUSE DICTIONARY OF THE ENGLISH LANGUAGE 1553 (2nd Ed. 1987). ("protection": "1. the act of protecting or the state of being protected; preservation from injury or harm."; "protect": "to defend or guard from attack, invasion, loss…; (continued...)

intersecting pixel activation lines." The term "row and column interconnections" does not appear to have antecedent basis and is ambiguous by itself, but from reading the remaining claim language and the specification, what is being removed are the lines/conductors that join the row lines together and the lines/conductors that join the column lines together. As disclosed in the specification, the pads of row/column lines "are serially connected together via jumpers outside of scribe lines 204 and 206," which are then "removed to provide the gate and source contacts" after "the back and front plans are mated." *See* '002 Patent at 8:7-8, 22-23 and 44-48.

7. **"inner electrostatic discharge guard ring" (claim 8)**

As explained above, the inner ESD guard ring differs from the outer ESD guard ring in that the inner ring can, under certain conduction, be an open L or C-shaped line, while the outer ring is strictly a surrounding structure. *See supra* at Section C.3. AUO therefore adopts CMO's construction for this term: "a closed or open ring, or open L or C-shaped conductive line, inside the active matrix display to provide…" *See* JCC, Ex. B, p. 12.

D. **U.S. Patent No. 5,825,449, "Liquid Crystal Display Device and Method of Manufacturing the Same"**

The '449 Patent relates to a process for fabricating a LCD device, specially the process for manufacturing the TFT panel of an LCD device. The embodiments disclosed in the '449 Patent teach different ways to interconnect TFT terminals (including gate, source, and drain) with wirings inside the TFT-array structure and to interconnect different layers of wirings provided near the periphery of the TFT-array structure.

1. **"formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer" / "overlying" (claim 1)**

AUO submits that this limitation should be construed as "produced above, supported by, and in contact with the second conductive layer and a second portion of the insulative layer covering the top surface of the first conductive layer" / "covering the top surface of." AUO's

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cover or shield from injury or danger.")

construction is consistent with the plain meaning of the term "overlying."[21] *See, e.g.*, Chen Decl., Ex. 5, RANDOM HOUSE WEBSTER'S COLLEGE DICTIONARY 931 (2nd Ed. 1997) ("overlie": "to lie over or on, as a covering or stratum.")

AUO's construction is further supported by the specification. *See* '449 Patent at Fig. 3 (element 9, the second insulative layer, is formed on element 3, the first insulative layer, which covers the top surface of element 2A). LGD's construction of "above" does not suggest the "covering" aspect of the plain meaning of this term, and it is therefore not as accurate as AUO's proposal.

2. **"one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor" (claim 1)**

AUO contends that this limitation should be construed as "at least one of the first and second conductive layers is electrically connected to at least one of the source, drain, and gate electrodes of a thin film transistor." LGD, on the other hand, proposes that this limitation be construed as "one, but not both, of the first and second conductive layers is directly connected to one terminal of a thin film transistor." The primary dispute between AUO's construction and LGD's construction is whether the limitation reads on a wiring arrangement whereby both the first and second conductive layer are respectively connected to a TFT terminal.[22]

a. **LGD's Proposal of the "one, but not both" Language Impermissibly Excludes the Embodiment Disclosed in the Patent Specification.**

LGD's proposed construction excludes the embodiment as shown in Figs. 4 and 5 of the '449 Patent. As discussed in the specification, Fig. 5 is a wiring structure (element 150 in Fig. 4) connecting the gate electrode and the source electrode of the transistor 160. '449 Patent at 5:23-38. In other words, the first and second conductive layers of the wiring structure are connected to two

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[21] AUO further notes that its construction for the term "formed on" is different from LGD's. This term is addressed globally along with the '737, '274, and '321 Patents above.

[22] We further note that LGD and AUO dispute the terms "connected to" and "terminals of a thin film transistor" within the context of this limitation as well.

of the terminals (the gate electrode and source electrode) of the thin film transistor 160. LGD's construction, therefore, would read out an embodiment disclosed in the patent, and is therefore improper. *Dow Chemical Co. v. Sumitomo Chemical Co.*, 257 F.3d 1364, 1378 (Fed. Cir. 2001).

b. **LGD's proposed construction is inconsistent with the remarks made by the Applicant during prosecution.**

The "wherein one of said first and second conductive layers is connected to one of a plurality of terminals of thin film transistor" limitation is also present in claim 6 of the '449 Patent (Claim 11 from the original application). The Applicant admitted, during the prosecution of the '449 Patent, that the first conductive layer in this clause could be embodied by a gate electrode, and the second conductive layer could be embodied by a source electrode. Joint Ex. C1 (file history for the '449 Patent), 12/01/97 Amendment at 5("[The] amended claim 11 essentially includes the recitations of canceled [dependent] claim 12 [which recites 'wherein said first conductive layer is a gate electrode and said second conductive layer is a source electrode']."). *See also id.* at 01/10/97 Application, p. 16. A gate electrode is part of the gate terminal of a TFT, and therefore is connected to the gate terminal. Likewise, a source electrode is connected to the source terminal. Thus, the wherein clause covers a structure where ***both*** the first conductive layer ***and*** the second conductive layer are connected to TFT terminals. LGD's proposal of "one, but not both" for the same clause from Claim 1 contradicts the Applicant's own remarks.

Finally, AUO's construction is consistent with the use of the open-ended term "comprising" in Claim 1. *See* MANUAL OF PATENT EXAMINING PROCEDURE Ch. 21, § 2111.03 (2007). It therefore follows that the "one of" limitation needs not be construed as restrictively as LGD's proposal requires. *E.g., Scanner Techs. Corp. v. ICOS Vision Sys. Corp.*, 365 F.3d 1299, 1304 (Fed. Cir. 2004).

3. **"gate pad"/ "source pad" (claims 10 and 11)**

AUO contends that these limitations should be construed as "a patterned, electrically conductive material provided near the periphery of the thin film transistor array to receive a gate/data signal from a gate/data driving circuit." LGD's proposal is "a portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array

to receive a gate/data signal." The disputes between the two parties' proposals are underscored.

While AUO's proposal is fully supported by the patent specification, LGD's proposal with respect to "a portion of" is unnecessary restrictive. The background section of the '449 Patent teaches that "gate pads and data pads are connected to the gate lines and data lines to receive data[s] from gate drive and data driver respectively." '449 Patent at 1:27-30. Figure 6, which shows a diagram of a TFT array viewed from the top, displays gate and sources pads as rectangles. There is no further division of these rectangles into smaller portions. There is therefore no teaching in the specification of dividing "patterned, electrically conductive material" into portions as gate and source pads.[23]

AUO's proposal further emphasizes that the gate/source pads receive signals from a gate/data driving circuit. The specification of the '449 Patent makes it clear that the gate and source pads receives data from "gate drive and data driver respectively." '449 Patent at 1:27-30. AUO's proposal adds clarity and completeness to the construction of the terms.

E. **U.S. Patent Nos. 5,905,274, 6,815,321, and 7,176,489, "Thin-Film Transistor and Method of Making Same"**

The '274, '321, and '489 Patents (collectively, the "'274 Patent Family") are aimed at structures of thin-film transistors containing double-layered gate electrodes and methods for fabricating such thin-film transistors. Specifically, the double-layered gate electrodes of the '274 Patent Family contain a layer of aluminum beneath a second overlying metal layer, the two layers having a stepped structure at their edges. This gate electrode structure overcomes the prior art problems of deterioration of step coverage by an overlying gate insulating layer, as well as preventing hillock formation in the bottom aluminum layer.

The '274 Patent specifically addresses the step coverage and hillock issues with double-layered gate electrodes. The '321 Patent issued from a divisional application within the family of

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[23] LGD's inclusion of the phrase "a portion" is also problematic because the meaning of the phrase is vague. Such proposal would not help the fact finder to determine the metes and bounds of the claim at issue.

applications originating from the application of the '274 Patent, and claims methods used to fabricate the structures claimed in the '274 Patent. The '489 Patent issued from a division of the application that resulted in the '321 Patent. The three patents contain the same disclosures.[24]

1. **"a double-layered structure" ('274 Patent, claims 1 and 4) / "[a] double-layered metal gate" ('321 Patent, claim 1) / "a double-layered metal gate" ('489 Patent, claim 1)**

AUO's proposed construction for the '274 term is "a two-layered step structure." AUO proposed that the '321 term be construed as "a gate electrode having a two-layered step structure." AUO further proposes that the '489 term be construed as "a gate electrode having a two-layered step structure."

This construction captures the key features of the gate structure that the inventors sought to claim: 1) it is composed of two layers; and 2) at their edges, the layers have a stepped structure with each other and with the substrate on which they rest.

a. **The "double-layered" structure contains two layers with a step structure at its edges.**

First, the inventors describe its invention a "gate 49 [having] a double-layered structure including ... ***first*** and ***second*** metal layers 43 and 45 disposed on the substrate 41." '274 Patent at 4:32-34 (emphasis added). Furthermore, the disclosed double-layer structure has an optimal "double step differences". It is optimal, according to the inventors, because it solves the two prior art problems that the inventors identify: too small a width differences between the first and second metal layers causes poor step coverage, which results in disconnections and short circuits, *see* '274 Patent at 1:45-60, and too large a difference causes hillock in the aluminum bottom layer, *see* '274 Patent at 2:17-20. *See also* '274 Patent at 2:55-60.

Furthermore, the inventors note that the prior art already describes structures where, like in the '274 Patent, a second metal layer is located on a first metal layer. *Id.* at 2:12-13. The key prior

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[24] The specification language of the '274, '321, and '489 Patents are substantially the same. Consequently, for the sake of convenience, citations used to support AUO's arguments that apply to all three patents in the '274 Patent Family will be to the specification of the '274 Patent, (continued...)

art references cited during prosecution, Wei and Miyago,[25] have similar double step structures. *See Kumar*, 351 F.3d at 1368. The '274 Patent Family does not purport to change this structure. The invention merely identifies a particular range of width differences that the inventors state are ideal in preventing defects, *see* '274 Patent at 4:39-44, 49-52, and is an improvement over prior art double-layered gate structures. *See id.* at 2:52-54.

b. **LGD's proposed construction does not accurately interpret the claim language.**

LGD proposes that this term be construed as "a structure of an electrically conductive material that includes two sequentially deposited metal layers." This construction improperly focuses on the method of fabricating the structure and ignores the patents' focus on the geometries of the structure. Indeed, the patentee explicitly chose not to prosecute the process claims for the '274 Patent. Joint Ex. F1 (file history for the '274 Patent), 7/24/98 Office Action; 8/10/98 Response to Restriction Requirement. Simply depositing two metal layers to obtain the step structure is not the focus of these patents. LGD's construction would ignore the very purpose of the invention.

2. **"the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first layer" ('274 Patent, claims 1 and 4)**

a. **"the sides" refers to the side portions of the first metal layer, and the disclosure only supports prevention of hillock at the top surface of those side portions.**

AUO's proposed construction for this term, which describes where hillock is prevented, is "at the portions on the top surface of the first metal layer not covered by the second metal layer." This construction is also consistent with the double-step structure that this invention was intended to work with, since such a structure would necessarily have side portions on the top surface of the first layer.

(...continued from previous page)
except where otherwise stated.

[25] *See* Chen Decl., Ex. 6 (the Wei Reference); Chen Decl., Ex. 7 (the Miyago Reference).

The inventors also identified too large width differences between the first and second metal layers as being the source of the problem of hillock formation in the aluminum bottom layer. *See* '274 Patent at 2:55-60. Because of this focus on width differences, it is apparent that the inventors were concerned about hillock formation along the lateral length of the exposed portions of the bottom aluminum layer. More particularly, the disclosures of the '274 Patent Family teach a structure that will prevent hillock formation along the exposed top surfaces of the exposed side portions of the first metal layer.

The "width," as used in the disclosures of the '274 Patent Family, refers to the top surfaces of the metal layers. *See*, *e.g.*, *id.* at 4:45-51; 5:34-38; 6:33-35. The inventors identify the "relationship between the width of the first metal layer and the width of the second metal layer" as "critical to preventing deterioration of step coverage." *Id.* at 4:40-45. Therefore, width must refer to the top surface portions of the first metal layer. *See also id.* at 4:53-58.

b. **LGD's proposed construction seeks to redefine the scope of the claim term.**

Essentially LGD tries to confuse the term "side/side portion" with "thickness" and proposes that this term be construed as "the second metal layer is patterned to prevent hillock on the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer." The patentee understood the differences between these two terms: "side/side portion" are used in the independent claims, while thickness is claimed in dependent claims 19-20 of the '321 Patent. The inventors focus on width differences, not thickness, as the key to the invention; LGD does not suggest how width differences relate to hillock occurring at side surfaces.

3. **"the first metal layer being wider than the second metal layer by about 1 to 4 μm" ('274 Patent, claims 1 and 4) / "the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm" ('321 Patent, claim 16) / "a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm" ('321 Patent, claim 7) / "a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm" ('489 Patent, claim 1)**

a. **The width terms are indefinite.**

AUO submits that these terms are indefinite because the disclosures of the '274 Patent

Family do not adequately teach how width of the two metal layers should be measured. One approach would be to measure the top surface of each of the first and second metal layers. See '274 Patent at Fig. 4C. Another approach would be to measure the top surface of the first metal layer that is not covered by the second metal layer, given the patents' focus on "double step differences." *Id.* at 5:25-8. In yet another alternative, the width of the first and second metal layers could arguably include sloped side portions, since the patents teach that "[t]he lateral surfaces of the second metal layer 45 are preferably etched to have a substantially rectangular or inclined shape." '274 Patent at 6:12-14. With no way to determine the correct measurement, the terms cannot be construed and are indefinite. *See Honeywell Int'l, Inc. v. ITC*, 341 F.3d 1332, 1340 (Fed. Cir. 2003) (finding claim indefinite when patent did not teach which of several tests to use to measure a numeric limitation).

b. **The width of the first metal layer should be defined by its top surface.**

If the Court does not believe that the patent is insolubly ambiguous, AUO proposes that the '274 term should be construed to mean "the first metal layer is about 1 to 4 μm greater than the width of the second metal layer measured from a level defined by the top of the first metal layer." AUO proposes that the '321 terms be construed as "the first metal layers being etched so that the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer" and "the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer," respectively. AUO further proposes that the '489 term be construed as "the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer measured from a level defined by the top of the first metal layer." These constructions clarify that width difference refers to the width of the top surface of the first metal layer, and is not measured where the possibly "inclined" ends of the first metal layer meets the substrate.

The specification language and corresponding figures of the '274 Patent Family relevant to

w1, the width of the first metal layer, and w2, the width of the second metal layer, consistently indicate what would seem to be the top surfaces of the two layers. In the specification, the width markings in Figures 3 and 4 indicate only the top surfaces. *See, e.g.*, '274 Patent at Fig. 4C. The claim language also seems to refer to the top surface, stating that "the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second layer thereon have the same width as each other." *Id.* at Claim 5.

Furthermore, the patents in the '274 Patent Family seem to teach obtaining a total top surface width of w1 for the first metal layer. *See id.* at 5:57-6:7 ("the width w1 of the photoresist 47 ... is the same as the width w1 of the first metal layer 43"). They also teach that the width of the second metal layer is equal to the width of the second photoresist: "The second photoresist 19 is exposed and developed so as to have a certain width w2 extending along the second metal layer 17 and located above the first metal layer 13." *Id.* at 1:61-65. Thus, the term should be construed to mean that width difference between the first and second metal layers indicates the width of the top surfaces of the uncovered side portions of the first metal layer.

Furthermore, in distinguishing prior art during the prosecution of U.S. Patent No. 6,573,127 (the "'127 Patent"), which discloses the same kind of double-layered gate structure as the '274 Patent Family, the inventors stated that the prior art references "do not teach or suggest a second metal layer formed only on a portion of the first metal layer, leaving two side portions on a horizontal upper surface of the first metal layer having no second metal layer formed thereon, as set forth in the presently claimed invention." Chen Decl., Ex. 8 (file history for the '127 Patent), 11/13/02 Amendment under 37 C.F.R. §1.111, p. 6.[26]

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[26] Application 10/872527, which issued as the '489 Patent, was initially rejected under obviousness-type double patenting in light of the '127 Patent. In distinguishing the teachings of the '127 Patent during the prosecution of the '489 Patent, the inventors simply stated that the '127 Patent contained only method claims, while the application of the '489 Patent "relate to the transistor itself, rather than the method of making the transistor." The inventors did not indicate that the teachings of the '489 Patent relating to the side portions of the first metal layer differed in any other way. Joint Ex. H1 (file history for the '489 Patent), 12/29/05 Response to Non-Final (continued...)

c. **LGD's proposed construction fails to provide any clarity to the term.**

LGD proposes that the term be construed to mean "the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4 μm greater than the width of the second metal layer." This construction does not resolve the ambiguity in the claim language, and imports a limitation about a subsequently deposited gate insulating layer. LGD fails to address how the width of the two metal layers, and consequently the width difference between them, should be measured.

F. **U.S. Patent No. 6,664,569, "Liquid Crystal Display Device Array Substrate and Method of Manufacturing the Same"**

The '569 Patent is directed to a specific type of layout structures for the TFTs in the array matrix, and claims several variations of such layout structures. In this particular type of layout structures, as exemplified in Figures 5-9, the TFT has specific configurations for its gate, source and drain electrodes. Specifically, a portion of the gate line is used as the gate electrode, and a rectangular or inverted "T"-shaped opening—formed by a cut out extending from the periphery of the gate line to interior—is created therein. *See, e.g.*, '569 Patent at Figs. 6A, 7 and 8; 6:31-41; 8:37-49; 8:63-66. Together, the layout structure of the special opening, a specific shaped drain electrode, a specially located semiconductor layer, and a substantially surrounding source electrode help to reduce and minimize the gate-drain parasitic capacitance. *See, e.g., id.* at Figs. 5-9; Abstract; 8:30-9:6.

1. **"a gate line" (claims 17 and 25)**

The term "gate line" should be construed as "an elongated directional conductor that supplies signals to gate electrodes." This construction is supported by the claim language, the plain meaning, and the specification of the patent.

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Office Action at 2.

As an initial matter, LGD's proposed construction completely ignores the plain meaning of "line"[27] and the corresponding description in the claims. As recited in the claims, a gate line is a "line arranged in a horizontal direction on a substrate" and crosses with the "data line" (*id.* at 9:22-27) and a gate line also "extend[s] along a first direction" (*id.* at 10:23-34, 63-64) and may "includ[e] a gate electrode" (*id.* at 10:64).[28] Second, the use of separate terms "gate line" and "gate electrode" in the claims of the '569 Patent suggests that they refer to separate components of a LCD device. Finally, the specification notes the distinction and is consistent with AUO's proposal in that a gate line "supplies signals to ***gate electrodes***." *See, e.g., id.* at Fig. 2, 2:23-25 ("gate line 13 supplies scanning signal to the gate electrode."); 2:63-65 (the gate electrode "protrude[s] from the gate line"). Because LGD's proposed construction defies plain meaning and is inconsistent with the specification, the Court should reject LGD's proposed construction.

2. **"the gate line having an opening therein" (claim 17) and "the gate electrode having an opening therein" (claim 25)**

As described in more detail below, LGD's proposed construction with respect to many of the disputed claim terms of the '569 Patent—e.g., "… having an opening therein," "the opening includes a first opening portion and a second opening portion," "a first electrode," "a second electrode," "a third electrode"—is to replace the structural limitations of the apparatus claim with functional limitations. *See* JCC, Ex. D. However, the rewriting of the apparatus claims in this manner is improper under Federal Circuit precedent and should not be allowed. *See Ecolab, Inc. v. Envirochem, Inc.*, 264 F.3d 1358, 1367 (Fed. Cir. 2001) (declining to import a functional limitation, even though the patentee noted the functional import of a structural phrase in the claim during prosecution). If LGD wanted to cover functional aspects of their patent, they should have written claims that recited the functional aspects of the device (e.g., method claims or means plus

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[27] *See* Chen Decl., Ex. 5, RANDOM HOUSE WEBSTER'S COLLEGE DICTIONARY 763 (2nd Ed. 1997) ("line": "2. a continuous extent of length, straight or curved, without breadth or thickness").

[28] The figures and specification further describe the gate line. *See* '569 Patent at Figs. 1, 2, 7, and 8; 2:23-25; 5:40-53; 8:37-42; 1:65-2:8; 2:63-65.

function claims).[29]

In light of the above proposed construction for "gate line" and "gate electrode," AUO submits that the phrase "the gate line/electrode having an opening therein" should be construed as "the gate line/electrode with a cut out extending from the periphery of the gate line to the interior of the gate line." AUO's construction recognizes the plain meaning of "an opening therein"[30] and is further supported by the specification. Each of the opening shown in the figures, either rectangular or inverted "T"-shaped, is a cut out from periphery of the gate line (*e.g.*, Figs. 5-8), and as the specification notes the cut out is "vertically elongated from a top edge to a center of the gate line." '569 Patent at 6:31-41. Having this cut out opening from the periphery is further consistent with the inventive aspect of having gate electrode overlap by only the edges of the drain electrode, and not at other portions of the drain electrode. *See, e.g., id.* at Abstract; 4:63-65; 6:13-15; 8:7-10; 7:6-18; 8:34-35; Fig. 8 ("overlapped area (depicted by oblique lines) is formed on both end sides of the drain electrode 117"). Only a cut out opening could allow for overlapping ***only*** at the edges of the drain electrode.

On the other hand, LGD seeks to improperly add functional limitations to an otherwise structure limitation, i.e., an opening in a gate line. Surprisingly, LGD failed to realize that the opening itself does not reduce gate-drain capacitance and compensate for gate-drain layer misalignment. The '569 Patent specifically teaches that such effect is, for example, achieved by overlapping the gate electrode only at the edges of the drain electrode and with surrounding source electrode along the steps of the semiconductor layer. *See, e.g., id.* at 7:18-23; 8:1-12.

Therefore, the Court should adopt AUO's proposed constructions.

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[29] The divisional patent to the '569 Patent, U.S. Patent No. 7,075,595, recites method claims. *See* Chen Decl., Ex. 9.

[30] *See* Chen Decl., Ex. 10, THE AMERICAN HERITAGE DICTIONARY OF THE ENGLISH LANGUAGE 1232 (4th ed. 2000) ("opening": "2. An open space serving as a passage or gap.").

3. **"the opening includes a first opening portion and a second opening portion," "a first opening portion," and "a second opening portion" (claim 25)**

Rejecting LGD's attempt to add functional limitations, the Court should construe the whole phrase, which include two sub-parts, as "non-rectangular-shaped opening having two distinct opening portions." While the specification specifically calls out a rectangle-shaped opening and an inverted "T"-shaped opening, it is clear that a rectangle-shaped opening does not have two separate and distinct opening portions. *See id.* at 8:40-45. The specification discusses in detail the first opening portion and the second opening portion of the inverted "T"-shaped opening. *See id.* at 4:48-53; 6:32-41; 7:6-19. Without limiting to the shape of the opening to an inverted "T"-shape, AUO's proposed construction captures the plain meaning and is consistent with the specification, including the non-rectangular shape and the two distinct opening portions.

4. **"a first electrode" (claim 25), "a second electrode" (claim 25) and "a third electrode" (claim 32)**

While both parties appear to agree that these "electrodes" represent three distinct portions of a "single" drain electrode, LGD's proposed constructions are again fraught with improper functional limitations. The Court should adopt AUO's proposed constructions, which track the plain meaning and are consistent with the specification to distinguish the three distinct portions. *See, e.g., id.* at Figs. 5, 6B, 6C, and 7-9; 4:53-60; 7:6-17; 6:6-12; 5:61-65; 7:29-32.

5. **"a semiconductor layer on the first insulating layer over at least a portion of the opening" (claim 7) and "a drain electrode on the semiconductor layer over at least a portion of the opening" (claim 17)**

One of the goals in claim construction is to provide clarity to the claim term, and AUO's proposed construction here does just that: "A semiconductor layer above, supposed by, and in contact with the first insulating layer, the semi-conductor layer being over at least a portion of the opening in the gate line" tracks the claim language and its plain meaning, making clear that the semi-conductor layer is over a portion of the opening. *See* JCC, Ex. D, p. 3. In contrast, LGD's construction is confusing, as either the semiconductor layer or the first insulating layer could be interpreted as the thing that "overlap[s]" the opening. *Id.* The specification provides ample support for AUO's clear construction, while providing none for LGD's construction if it is

requiring the insulator layer to overlap the opening. *See, e.g.*, '569 Patent at Figs. 6A, 8 and 9; 6:47-54 ("[I]n Fig. 6A, the semiconductor layer 123 is located over the inverted 'T'-shaped opening 114 of the gate electrode 115…"). The Court, therefore, should adopt AUO's proposed construction.

Consistent with the rationale set forth above, the plain meaning of the claim language directs the construction of "a drain electrode on the semiconductor layer over at least a portion of the opening" (claim 17) to be the one proposed by AUO. *See* JCC, Ex. D, p. 4. This construction is similarly supported by the specification. *See, e.g.*, '569 Patent at Figs. 6A, 8 and 9 (element 117a is the drain electrode, element 123 is the semiconductor layer); 7:48-51, 7:6-20.

6. **"substantially surrounds the drain electrode" and "substantially" (claim 21)**

AUO's proposed construction for this phrase, with the sub-part "substantially," is "surrounds almost all the drain electrode portion." The dispute between the parties appears to be between LGD's "extending considerably around" and AUO's "surrounds almost all." Based on the plain meaning of "surround" to mean "to enclose on all sides"[31] and the specification, it is clear that AUO's construction is more appropriate. "Surrounds almost all" better captures the plain meaning of "substantially" enclosing on all sides. The figures related to the '569 invention, i.e., Figs. 5, 6B, 6C, 7 and 8, further support a source electrode 119 that surrounds almost all the drain electrode portion. *See also id.* at 4:37-40; 5:53-61; 6:66-7:2; 7:18-23, 8:5-7.

G. **U.S. Patent No. 6,803,984, "Method and Apparatus for Manufacturing Liquid Crystal Display Device Using Serial Production Processes"**

The '984 Patent relates to the method for manufacturing an LCD device in a single production process line starting from processing the two opposing substrates of the LCD devices to assembling them together, rather than using two parallel production processing lines or branching into such parallel processing during manufacturing. At all times, this single line structure is

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[31] *See* Chen Decl., Ex. 11, RANDOM HOUSE WEBSTER'S UNABRIDGED DICTIONARY 1916 (2nd Ed. 2001) ("surround": "1. to enclose on all sides; encompass. 2. to form an enclosure round; encircle.")

maintained when progressing, in serial order, each alternate pair of the top and bottom substrates for processing by the different equipment/machines. *See, e.g.* '984 Patent at Figs. 2-4; 5:23-30; 7:35-41; 3:61-4:48. The claimed invention makes clear that both pair of the substrates must pass through the equipment/machine for coating the sealing material with one of them not being processed on, and that both pair of the substrates must also pass through the equipment/machine for dispensing the liquid crystal with one of them not being processed on. *See, e.g., id.* at 7:62-8:8.

1. **"on a single production process line" (claim 1)**

AUO's proposed construction for this term is "on a production line for processing liquid crystal displays in a single, linear arrangement," which flows directly from ordinary meaning of the claim language and is further consistent with the specification. JCC, Ex. E, p. 2. Plaintiff's proposed construction, on the other hand, seeks to improperly add limitations--e.g., "processing equipment [] arranged along a common path"--without logic and in contradiction with the specification and patentee's arguments during prosecution to overcome prior art.

AUO's construction reflects the spatial arrangement, i.e., single line, and processing flow, of a linear arrangement (as opposed to parallel processing). *See, e.g.*, '984 Patent at Figs. 2-4; 7:35-41; 5:23-30; 3:24-42. AUO's construction is also supported by the specification, which indicates that the two opposing substrates are alternatively provided into "a production line having a single line structure for progressing the liquid crystal cell process." *Id.* at 5:23-27. The plain meaning of "production line"[32] and the remaining claim language further dictate the "single, linear arrangement" so that both opposing substrates will pass under a sealing material coating and a liquid crystal dispensing equipment/machines in serial order, rather than through "two separate and parallel" lines. *See id.* at 7:58-8:11; *see also id.* at 3:24-42.

On the other hand, LGD's proposed construction of "on a production line where the processing equipment is arrange along a common path for performing the liquid crystal cell

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[32] *See* Chen Decl., Ex. 11, RANDOM HOUSE WEBSTER'S UNABRIDGED DICTIONARY 1544 (2nd ed. 2001) ("production line": "an arrangement of machine or sequence of operations involved with a (continued...)

process" contradicts the intrinsic evidence. First, the specification does not describe that the processing equipment can be arranged "along a common path," meaning that the processing equipment can sit on either side of this path. Interpreting the term this way would allow for parallel or non-linear processing and create multiple production lines when, for example, the sealing material coating machine and the liquid crystal dispensing machine are placed opposite each other on the common path, with one machine on one side and the other machine on the other side. The two machines would then be parallel with each other along this common path. However, the specification discloses the claimed "single production process line" as having "a single line structure" and is used to "overcome problems caused by" having two parallel processing. *See id.* at 5:23-25; 7:35-42; 3:25-43. Moreover, the patentee overcame prior art, JP8-171076, by specifically disclaiming such parallel arrangement. During prosecution, the patentee argued that while the Japanese reference does show single processing line for carrying out "common processing…when the same processes are desired," multiple processing lines are branched out from the single process line at later stages for "parallel processing…when distinct processes are desired." Joint Ex. E1 (file history for the '984 Patent), 1/8/04 Amendment, p. 4-5. Because LGD's construction allows processing equipment to be arranged along a common path on either side, it encompasses the prior art. *See* Chen Decl., Ex. 12, JP8-171076, Abstract; Fig. 3 (parallel treatment stages 19, 20 sit parallel to each other along a common path). The Court should therefore adopt AUO's construction.

2. **"passing the first and second substrates through a sealing material coating portion of the single production process line in serial order" and "a sealing material coating portion of the single production process line" and "in serial order" (claim 1)**

AUO construes the whole limitation, which encompasses the two subparts, as "providing the first and second substrates one after the other, without anything in between; in at one end, and out at the other end in the same order of a equipment/machine for coating sealing material on a

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single manufacturing operation or production process.").

substrate in the single production process line." JCC, Ex. E, pp. 3-5.

AUO's proposed construction adds clarity to the claim language by further illustrating the ordinary meaning of "passing through" and "in serial order."[33] In the context of the claim language and the patent as a whole, it is clear that the first and second substrates are provided one after the other, without anything in between, and that the two substrates goes in at one end, and out at the other end in the same order of a equipment/machine for coating sealing material on a substrate in the single production process line.

AUO's proposed construction is consistent with the specification. Figures 2-4 each show that first and second substrates are provided without anything in between. The first substrate ("TFT substrate") and the second substrate ("color filter substrate") are "alternately provided into a production line." '984 Patent at 5:23-30. This alternate arrangement dictates that nothing be between the first and second substrate. The summary of invention further describes the process of the sealing coating equipment/machine "receiv[ing] the first and second substrates in serial order" for processing, after which the liquid crystal dispensing equipment/machine "receive[s] the first and second substrates in serial order," which requires the two substrates go in at one end of the sealing coating equipment/machine, and then out at the other end in the same order. *Id.* at 4:14-25; *see also id.* at 6:19-41. The patent further describes processing the first and second substrate as a "pair," with "each pair pass[ing] through each component of production process line." *Id.* at 7:25-33. These "components" of the production process line, as used in the '984 Patent, are the "processing equipment/machines" that the pair of opposing substrates are "provided to" so that processes associated with them are carried out in the "equipment/[machine] for the TFT substrate, equipment/[machine] for the color filter substrate or both." *Id.* at 5:26-30.

On the other hand, LGD's proposed construction improperly changes "passing through" to

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[33] *See* Chen Decl., Ex. 13, THE OXFORD AMERICAN COLLEGE DICTIONARY 1249 (2002) ("serial": "1. consisting of, forming part of, or taking place in a series"; "series": "a number of things...of a similar kind or related nature coming one after another.").

"passing" and merely paraphrases the claim term, rather than clarifying the ambiguity. Therefore, the Court should adopt AUO's proposed construction.

3. **"passing the first and second substrates through a liquid crystal dispensing portion of the single production process line in serial order" (claim 1)**

Consistent with the rationale set forth in the previous section, the Court should also adopt AUO's construction for this similar term. *See* JCC, Ex. E, p. 5. Here, the liquid crystal dispensing equipment/machine "receive[s] the first and second substrate in serial order" and process them, and then assembler "receive[s] the first and second substrate" in the same order. *See* '984 Patent at 4:20-30.

4. **"the liquid crystal is dispensed onto the first substrate at the same time the second substrate is disposed in the sealing material coating portion" (claim 5)**

AUO's construction is "when the liquid crystal is dispensed onto the first substrate in the liquid crystal dispensing equipment/machine, the second substrate is located in the sealing material coating equipment/machine." *See* JCC, Ex. E, p. 7.

The dispute here centers on whether the claim term requires only "overlap" in time. However, this proposed construction of LGD does not reflect the ordinary meaning, as the claim term is "at the same time," not merely "overlap in time." These two terms have different meaning, and merely requiring "overlap in time" unnecessarily broaden the claim scope.

In contrast, AUO's construction is consistent with the ordinary meaning of "at the same time"[34] and the specification, which clearly requires processing at the same time, so that when the liquid crystal is dispensed onto the first substrate in the liquid crystal dispensing equipment/machine, the second substrate is located in the sealing material coating equipment/machine to be processed. *See* '948 Patent at 7:22-33.

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[34] *See* Chen Decl., Ex. 13, THE OXFORD AMERICAN COLLEGE DICTIONARY 1201 (2002) ("at the same time": "simultaneously").

5. **"cleaning the first substrate and second substrate in serial order in a same cleaning unit" (claim 10)**

Consistent with the discussions in Section G.2 on "in serial order," AUO submits that the construction for this term should include the description "without anything in between" because it provides further clarity to the claim term. *See* JCC, Ex. E, p. 7. There appears to be no other dispute between the parties' proposed constructions. Once again, the first and second substrates are "alternately provided into a production line" and provided as "pair", *See* '984 Patent at 5:23-30; 7:25-34, and then cleaned in the same cleaning machine in serial order. *See id.* at Figs. 2-4; 5:33-41; 6:20-27. Afterwards, the first and second substrate pair is received by the next machine on the production line in serial order. *Id.* The Court, therefore, should adopt AUO's proposed construction.

H. **U.S. Patent No. 7,218,374, "Liquid Crystal Display Device and Method of Manufacturing the Same"**

The '374 Patent discloses a technique to apply a specific sealant pattern during the fabrication of a LCD panel, and claims a method of manufacturing a LCD device utilizing such a technique. As the patent explains, the disclosed technique dispenses sealant material outside the main region first (70a), and continues dispensing the rest to make an enclosure (70b) (element 50 is liquid crystal). '374 Patent at 5:3-20; Figs. 3B and 3C. By starting out the sealant application from outside the square (70b), the first drop of the sealant, which often deposit in the shape of a big blob (the starting point of 70a), would not come into contact with the liquid crystal in the finished panel product. Sealant contamination is therefore prevented. *See* '374 Patent at 2:39-54.

1. **"forming a main sealant/main sealant" (claim 1)**

AUO submits that this limitation should be construed as "forming a segment of sealant that encloses the liquid crystal in the LCD panel" / "a segment of sealant for enclosing the liquid crystal in the LCD panel." AUO's construction is supported by the specification of the patent, and also consistent with the plain meaning of the terms.

LGD's construction is "sealant material that encloses the display region." Both AUO and LGD agree that the main sealant performs an "enclosing" function. *See* '374 Patent at Fig. 3B

(element 70b constitutes the main sealant). AUO and LGD's proposal differ, on the other hand, on whether (1) the main sealant is just a "segment of sealant," and (2) what is being enclosed by the "main sealant."

With respect to the first difference, the sealant pattern disclosed in the '374 Patent shows that it contains segmented sealing material; one segment is used to enclose the liquid crystal, *see id.* Fig. 3B (70a), and the remaining segment is outside the enclosure defined by the first segment. *See id.* at Fig. 3B (70b). This dichotomy between the main and auxiliary sealant is maintained throughout the patent specification. *E.g.*, *id.* at 5:7-20.

With respect to the second difference, AUO's construction is clearly supported by the specification, and is also consistent with the understanding by one of ordinary skill in the art of the function of sealant. The '374 Patent, for example, describes the main UV sealant's function as "confin[ing] the liquid crystal." *Id.* at 3:20-24. It further noted that "prevent[ing] the liquid crystal from leaking out" is the ordinary function of a sealant. *Id.* To state the function of the main sealant as enclosing "the display area," as what LGD's proposal requires, is therefore imprecise and inaccurate.

2. **"a dummy region" (claims 1 and 21)**

AUO believes that this limitation should be construed as "an area outside the enclosure of the main sealant." While LGD's construction, which states "an area outside of the main sealant," appears to agree with AUO's proposal in spirit, AUO submits that its proposal is more precise and accurate. According to AUO's proposal, there are two areas: one area is defined by what main sealant encloses; the other area is outside such enclosure. AUO construction has ample support in the specification. *See id.* at 2:48-50; Figs 3 & 4. In contrast, LGD's construction is inadequate because "main sealant" does not define a region.

3. **"auxiliary sealant" (claim 1)**

AUO submits that this limitation should be construed as "a segment of sealant that extends from the main sealant and is outside the enclosure of the main sealant." AUO's construction is supported by the specification of the patent. Again, LGD's construction is "sealant deposited in an

area outside of the main sealant." The differences between AUO and LGD's proposals are (1) whether the auxiliary sealant is a segment of sealant, (2) whether it "extends from" the main sealant, and (3) whether it is "outside the enclosure of the main sealant." The first and last issues are addressed above, leaving issue (2) to focus upon.

The claim language, the patent specification, and the file histories all require that the recited auxiliary sealant "extends from" the main sealant. *See id.* at Claim 1 ("… wherein the auxiliary sealant is formed in a dummy region and connects to the main sealant, and wherein the auxiliary sealant and the main sealant are contiguous."); Claim 21 ("… wherein the auxiliary sealant is formed in a dummy region and extends outside from the main UV sealant, wherein the auxiliary UV sealant contacts the main UV sealant."); Figs. 3B and 3C (70a extends from 70b). *See also* Joint Ex. I1 (file history for the '374 Patent), 2/4/04 Amendment in Response to Non-Final Office Action, pp. 7-8 (Claim 1 is distinguishable over prior art because "neither references teaches an auxiliary sealant connecting to a main sealant"); pp. 8-9 (Claim 21 is distinguishable over prior art because "neither references teaches an auxiliary UV sealant extending from a main UV sealant"); 7/15/04 Reply under 37 C.F.R. § 1.111, pp. 2-3 (similar remarks).

Further, the purpose of the alleged invention requires that the auxiliary sealant be applied contiguously with the main sealant. If there is a break during the process, then the patent would not solve the problem it attempts to fix: contamination by sealant material of liquid crystal due to the big-blob formed when the dispenser first starts application. *See* '374 Patent at 2:41-55.

V. CONCLUSION

AUO respectfully requests that the Court adopt the claim constructions it has proposed above and in the Joint Claim Construction Chart at D.I. 376.

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CERTIFICATE OF SERVICE

I, Andrew A. Lundgren, Esquire, hereby certify that on August 11, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to the following counsel of record:

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Exhibit A

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1: A process for producing a thin-film transistor comprising	a process for producing a thin-film transistor (C)		a method for manufacturing thin-film transistors such as for a liquid crystal display	plain meaning in light of the construction below for "thin-film" transistor	plain meaning
	thin-film transistor (C)	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	Plain meaning. Alternate: A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
a first step for forming a gate electrode on an insulating substrate,	forming a gate electrode on an insulating substrate (C)		giving form or shape to a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode that is above and supported by or in contact with material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation	plain meaning	Producing a gate electrode above, supported by, and in contact with an insulating substrate
	forming ... on (C)	"Giving form or shape to . . . above and supported by or in contact with."	giving form or shape to...above and supported by or in contact with	plain meaning	Producing . . . above, supported by, and in contact with
	insulating substrate (C)	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation. [Previously Agreed upon Construction]	the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical	The material (such as glass, quartz, ceramic, insulator-coated silicon or insulator-coated metal) upon which the transistor is fabricated to provide mechanical support and electrical

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			insulation.	insulation	insulation
a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere,	continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film (C)	"on said gate electrode and substrate" – Above and supported by or in contact with the gate electrode and the insulating substrate. [Previously Agreed upon Construction]	the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film (without intervening films) above and supported by or in contact with (i) the patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode and (ii) the material (such as glass, quartz, ceramic, insulator-coated silicon or insulator coated metal) upon which the transistor is fabricated to provide mechanical support and electrical insulation.	construe the term: "depositing on said gate electrode and substrate" as: depositing above and in contact with the gate electrode and the insulating substrate	Precipitating a gate insulating film, a high resistivity semiconductor film and a conductive film on the gate electrode and the substrate without intervening films in between.
	continuously depositing (L, C, A)	"The formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films."	the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films	The formation of the gate insulating film, the high-resistivity semiconductor film and conducting film without intervening films.	Precipitating… without intervening films

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
	depositing on (C)		the formation of the gate insulating film the high-resistivity semiconductor film and conducting film above and supported by or in contact with	this term should be construed as part of the larger term "depositing on said gate electrode and substrate"	Precipitating above, supported by and in contact with
	depositing (A)		the formation of the gate insulating film, the high-resistivity semiconductor film and conducting film	Plain meaning	precipitating
	gate insulating film (C)		a thickness of non-conductive material (such as SiNx) that has a high electrical resistance and insulates the transistor gate from the semiconductor.	a thickness of material (such as SiNx, SiOx, or a multi-layer film made of such materials) with a high electrical resistance, spanning the region from the gate electrode to the high resistivity semiconductor layer, for insulating the gate electrode from the channel	plain meaning or insulating film formed over the gate region
	high-resistivity semiconductor film (C)	"A thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline	a thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen- fluorine	A thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine	Plain meaning or Semiconductor having the property of high resistivity

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
		amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film"	alloy, or a microcrystalline amorphous silicon) that has a higher resistance to current flow relative to the low-resistivity semiconductor film.	alloy, or a microcrystalline amorphous silicon) that has a high resistance to current flow and acts as the channel region of the transistor	
	conducting film (C)	"A thickness of electrically conductive material."	a thickness of electrically conductive material	A thickness of electrically conductive material that lies adjacent to the channel layer	plain meaning
	[a] conducting film containing at least a low-resistivity semiconductor film (L, C, A)	"The conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films."	the conducting film is composed of a low-resistivity semiconductor film and possibly other conductive films	Plain meaning The terms "conducting film" and "low-resistivity semiconductor film' should be construed separately from this term.	plain meaning
	low-resistivity semiconductor film (C)	"A thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon, which contains phosphorous or other impurities to enhance the conductivity	a thickness of semiconductor material (such as low-resistivity amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon which contains	A thickness of semiconductor material (such as amorphous silicon, hydrogenated amorphous silicon, amorphous silicon-fluorine alloy, amorphous silicon-hydrogen-fluorine alloy, or a microcrystalline amorphous silicon) that has a low	Plain meaning or semiconductor having the property of low resistivity

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
		of the film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film."	phosphorous or other impurities to enhance the conductivity of the film) that has a lower resistance to current flow relative to the high-resistivity semiconductor film.	resistance to current flow	
	without exposing them to an oxidizing atmosphere (C)		without exposing the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film to an atmosphere that would create a detectable amount of oxidation on a film.	Without permitting the gate insulating film, high-resistivity semiconductor film, low-resistivity semiconductor film, or conducting film to come into contact with an uncontrolled ambient atmosphere which contains oxidizing agents	Without exposing them to an atmosphere containing an oxidizing agent
	them (C)	The gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film. [Previously Agreed upon Construction]	the gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film.	The gate insulating film, the high-resistivity semiconductor film, and the conducting film containing at least the low-resistivity semiconductor film	indefinite
	oxidizing atmosphere (C)	"An atmosphere that would create a detectable amount of oxidization on a film."	an atmosphere that would create a detectable amount of oxidation on a film.	an uncontrolled ambient atmosphere which contains oxidizing agents	atmosphere containing oxidizing agent
a third step in which	selectively etched (C)	"The removal of selected	The removal of	Plain meaning	Selectively removed

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode,		portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface."	selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.		or corroded by a chemical agent
	they are partly left as an island region on said gate electrode (L)		a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor	Plain meaning	indefinite
	island region on said gate electrode (C)	"Portion of the conducting film, low-resistivity semiconductor film and high-resistivity semiconductor film which has been etched around its entire perimeter into a separate isolated region located over the gate electrode of a single thin-film transistor."	a portion of the high resistivity semiconductor film and conducting film has been etched around its perimeter into a region located over the gate electrode of a thin-film transistor.	Plain meaning	Isolated region above, supported by, and in contact with the gate electrode
	gate electrode (C, A)	"A patterned, electrically conductive material that controls current flow through the channel	a patterned electrically conductive material that controls current	A patterned electrically conductive material that controls current	A patterned, electrically conductive material formed in the gate

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
		between the source electrode and the drain electrode."	flow through the channel between the source electrode and drain electrode	flow through the channel between the source electrode and drain electrode.	region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other	a fourth step for selectively forming a source electrode and drain electrode (C, A)	"Forming a source electrode and drain electrode in selected regions only. Court noted that 'source and drain electrodes can be formed via deposition and subsequent etching of conductive material."	forming a source electrode and drain electrode in selected regions only	Plain meaning	Step-plus function element. Function is "selectively forming a source electrode and drain electrode
	selectively forming (C)	"Forming in selected regions only."	forming in selected regions only	Plain meaning	selectively producing
	source electrode (C, A)	"A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode."	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	construe term: "a source electrode and a drain electrode" as: Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
				the drain electrode of the transistor under control of the gate electrode of the transistor.	
	drain electrode (C, A)	"A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode."	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode.	this term should be construed as part of the larger term "a source electrode and a drain electrode"	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
	contacting a part of the surface of said island region (L, C)	"Touching a part of the surface of the island region."	touching a part of the surface of the island region	Touching a part of the surface of the island region.	plain meaning
a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask,	a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask (A)		a fifth step for removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask wherein the source electrode and drain electrode serve as at least a part of the pattern above a surface from which material is to be selectively removed;	eliminating all the conducting film in the space between the edges of the source and drain electrodes	a fifth step for using the source and drain electrodes to partially define the boundary for the removal of the conducting film exposed on the island region

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			the pattern is made of material that is resistive to the removal technique relative to the material to be removed		
	selectively removing said conducting film exposed on said island region (C)		removing selected regions only of the conducting film on the island region not covered by the source electrode, drain electrode or mask	eliminating all the conducting film in the space between the edges of the source and drain electrodes	plain meaning
	selectively removing (C)	"Removing selected regions only."	removing selected regions only	This term should be construed as part of the larger term, "selectively removing said conducting film exposed on said island region."	plain meaning
	said conducting film exposed on said island region (A)		the conducting film on the island region that is not covered by the source electrode, drain electrode or mask	Plain meaning	the conducting film on top of the island region is exposed to the atmosphere
	[said] source and drain electrodes serving as at least a part of the mask (C, A)		the source and drain electrodes serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that	The source and drain electrodes are part of the pattern on the top surface that protects underlying layers from being removed while allowing the portion of the layer exposed between the	Using the source and drain electrodes to partially define the boundary for the removal or formation of the conductive film

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			is resistive to the removal technique relative to the material to be removed	source and drain electrodes to be removed	
	serving as at least a part of the mask (L)		serving as at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask" see also construction of "mask" below	using … to partially define the boundary for the removal process
	at least a part of the mask (C)		at least a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of material that is resistive to the removal technique relative to the material to be removed.	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask"	to partially define the boundary for the removal or formation process
	a part of the mask (A)		a part of the pattern above a surface from which material is to be selectively removed, where the pattern is made of	this term should be construed as part of the term "said source and drain electrodes serving as at least a part of the mask"	to partially define the boundary for the removal or formation process

	U.S. Patent No. 4,624,737 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			material that is resistive to the removal technique relative to the material to be removed.		
	mask (A)	"a pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to material to be removed."	A pattern above a surface from which material is to be selectively removed. The pattern is made of material that is resistive to the removal technique relative to the material to be removed.	A top surface pattern above one or more layers of material that will be selectively removed according to the shape of the mask. The mask is made of material that is resistive to the removal technique and defines by its edges the boundaries of the material selected for removal.	A pattern to define the boundary for the removal or formation process.
a sixth step for depositing a surface passivation film, and	surface passivation film (C)	A thickness of material that provides protection such as electrical stability and chemical isolation. [Previously Agreed upon Construction]	a thickness of material that provides protection such as electrical stability and chemical isolation.	Plain meaning	plain meaning
a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.	exposing a part of each of said source electrode, drain electrode and gate electrode (C, A)		removing portions of one or more layers to uncover a part of each of said source electrode, drain electrode and gate electrode	Plain meaning	causing a part of the source electrode, drain electrode and gate electrode to be exposed to the atmosphere
	exposing (A)		removing portions of one or more layers to uncover		Uncovering

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1: A method of manufacturing active matrix display backplanes and displays therefrom, comprising:					
providing a substrate;	Substrate (C)		the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	Plain meaning	plain meaning
forming a pattern of pixels on said substrate;	forming a pattern of pixels on said substrate (C)		depositing and etching a matrix of transparent electrically conductive material to form pixel electrodes above and supported by or in contact with the substrate	Forming a repeating configuration of redundant subpixels.	Forming a pattern of pixels above, supported by and in contact with the substrate
forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;	forming a plurality of row and column intersecting pixel activation lines (C)		depositing and etching electrically conductive material patterned in rows and columns that control pixels	Forming a plurality of row intersecting pixel activation lines and column intersecting pixel activation lines	forming a plurality of row intersecting pixel activation lines and a plurality of column intersecting pixel activation lines
	interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another (A)		electrically connecting with conductive material all or nearly all row lines to at least one other row line and electrically connecting with conductive material all or nearly all	Electrically connecting with conductors nearly all, but not all, of said row lines to one another and nearly all, but not all, of said column	joining almost all of the row lines together and joining almost all of the column lines together

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			of the column lines to at least one other column line	lines to one another.	
	Interconnecting (L, C)	"Electrically connecting with conductors"	electrically connecting with conductive material	Electrically connecting with conductors.	joining together
	substantially all (C, A)		all or nearly all	Nearly all, but not all.	almost all
	row lines (C)		electrically conductive material patterned in rows that control pixels	Indefinite or lines connecting all pixels in a row	indefinite; or lines connecting all pixels in a row
	Column lines (C)		electrically conductive material patterned in columns that control pixels	indefinite or lines connecting all pixels in a column	indefinite; or, lines connecting all pixels in a column
	row and column lines (C)		electrically conductive material patterned in rows and columns that control pixels	Indefinite or the row lines and the column lines	indefinite; or the row lines and the column lines

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and	outer electrostatic discharge guard ring (L, C, A)	"A closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges."	a closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharge	A closed or open ring, or open L or C-shaped line, outside the active matrix display to provide protection from electrostatic discharges.	A surrounding structure outside the active matrix display to provide protection from electrostatic discharges
	resistance (L, C, A)	"A circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from electrostatic discharge."	a circuit component designed to provide opposition to electric current flowing through itself and to minimize current surge in the TFT array from electrostatic discharge	A circuit component that has a specified resistance to the flow of electric current and is used to minimize the current surge from an electrostatic discharge.	A circuit component that has a large[1] specified ratio between voltage and the flow of electric current, and used to minimize the current surge from electrostatic discharge.
	to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays (A)		to minimize current surge in the TFT array from electrostatic discharge during manufacture of the display	Indefinite	To guard against electrostatic discharges between the row activation lines and column activation lines during the manufacturing of the displays
	protection from electrostatic discharges (C)		to minimize current surge in the TFT array from electrostatic discharge during manufacture of the	Indefinite	Plain meaning; or Guarding against

[1] Due to a clerical error, the word "large" was inadvertently omitted from the previously submitted JCC. It is herein reinserted.

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			display		electrostatic discharges
	row and column activation lines (C)		electrically conductive material patterned in rows and columns that control pixels	indefinite or control lines activating all pixels in rows and control lines activating all pixels in columns	Indefinite; or Control lines activating all pixels in rows and control lines activating all pixels in columns.
removing said outer guard ring and row and column interconnections prior to completion of the display.	removing said outer guard ring and row and column interconnections (L, C)	"Physically disconnecting said guard ring and row and column interconnections"	physically disconnecting said guard ring and row and column interconnections	Physically disconnecting said guard ring and row and column interconnections.	Indefinite; Or physically disconnecting said guard ring and lines connecting the row and column intersecting pixel activation lines from the substrate
	Removing (A)		physically disconnecting said guard ring and row and column interconnections	Physically disconnecting	Taking away Alternate 1: separating or breaking off Alternate 2: physically disconnecting
Claim 8: The method as defined in claim 1 including forming an inner electrostatic	inner electrostatic discharge guard ring (L, C)		a closed or open ring, or open L or C-shaped line, inside the source and/or gate pads to	A closed or open ring, or open L or C-shaped conductive line,	Ring structure inside the active matrix display to provide protection from

	U.S. Patent No. 5,019,002 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.			provide protection from electrostatic discharge	inside the active matrix display to provide protection from electrostatic discharges.	electrostatic discharges
	shunt switching element[s] (L, C, A)		shunt transistors, including floating gate, no gate, an oxide below to form a spark gap, or other active switching elements such as diodes	An active switching element like a shunt transistor or diode.	A switching circuit for shunting electrostatic discharges

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1. A wiring structure comprising:	wiring structure (C)	A structure providing an electrically conductive path that connects at least two terminals.	a structure electrically connecting at least two points	A structure providing an electrically conductive path that connects at least two terminals.	a structure made by wires
a substrate;	Substrate (C)	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support. [Previously Agreed upon Construction]	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
a first conductive layer formed on a first portion of said substrate;	conductive layer (L, C)	A thickness of electrically conductive material. [Previously Agreed upon Construction]	thickness of electrically conductive material	A thickness of electrically conductive material that may include one or more patterned features, all of a single material.	plain meaning
	layer (C)		a thickness of material	plain meaning	plain meaning
	formed on a first portion of said substrate (C)		above and in contact with a first part of the substrate	above and in contact with a first part of the substrate	Produced above, supported by, and in contact with a first portion of the substrate
	formed on (C, A)	Formed "above and supported by or in contact with."	above and in contact with	above and in contact with	Produced above, supported by, and in contact with

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
a first insulative layer formed on a second portion of said substrate and on said first conductive layer;	formed on a second portion of said substrate (C)		above and in contact with a second part of the substrate	above and in contact with a second part of the substrate	Produced above, supported by, and in contact with a second portion of the substrate
a second conductive layer formed on a first portion of said first insulative layer;	formed on a first portion of said first insulative layer (C)		above and in contact with a first part of the first insulative layer	above and in contact with a first part of the first insulative layer	Produced above, supported by, and in contact with a first portion of the first insulative layer
	insulative layer (C)	A thickness of non-conductive material (such as SiNx) that has high electrical resistance. [Previously Agreed upon Construction]	a thickness of non-conductive material (such as SiNx) that has high electrical resistance.	Plain meaning	plain meaning
a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;	formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer (C)		above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer	above and in contact with the second conductive layer and above and in contact with a second part of the first insulative layer above the first conductive layer	Produced above, supported by, and in contact with the second conductive layer and a second portion of the insulative layer covering the top surface of the first conductive layer
	Overlying (C, A)	Above [Previously Agreed upon Construction]	above	this term should be construed as part of the larger term ("formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer"	covering the top surface of

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
an indium tin oxide layer formed on said second insulative layer,	indium tin oxide layer (C)	A thickness of indium tin oxide (ITO). [Previously Agreed upon Construction]	A thickness of indium tin oxide (ITO).	A thickness of indium tin oxide (ITO).	A thickness of indium tin oxide (ITO).
wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and	contact hole is provided through ... layer[s] (C, A)	"The contact hole is formed in the layer."	the contact hole is formed in the layer	the contact hole is formed in the layer(s)	The contact hole is formed in the layers
	contact hole (C)	an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection. [agreed upon]	an opening in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.	An opening formed in one or more insulative layers to expose a portion of a conductive layer for purposes of forming an electrical connection.	plain meaning
	provided through (C)	*see* construction for "contact hole is provided through . . . layer"	the contact hole is formed in the layer	Plain meaning.	see above
	expose part of said ... layer (C)		removing portions of one or more layers to uncover at least part of another layer	Plain meaning	plain meaning
	extends through (C)		is disposed in	Plain meaning	plain meaning
	electrically connect ... with (C)		provide an electrical conduction path between the first and second conductive layers	plain meaning	plain meaning

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.	one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor (C, A)		one, but not both, of the first and second conductive layers is directly connected to one terminal of a thin film transistor	The first conductive layer is connected to the gate, source or drain of a thin film transistor, and/or the second conductive layer is connected to the gate, source or drain of the thin film transistor.	At least one of the first and second conductive layers is electrically connected to at least one of the source, drain, and gate electrodes of a thin film transistor.
	one of said first and second conductive layers (C)		one, but not both, of the first and second conductive layers	this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor"	at least one of the first and second conductive layers
	one (L)	The court construed "one of" as "one, but not both, of the first and second conductive layers."	A single layer	This term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor."	plain meaning
	connected to (C, A)		directly connected to	Plain meaning	Electrically connected to
	one of a plurality of terminals of a thin film transistor (L)	One of the terminals (i.e., source, drain, or gate) of a thin film transistor. [Previously Agreed upon Construction]	one of the terminals (i.e., source, drain, or gate) of a thin film transistor	This term should be construed as part of the larger term "one of said first and second conductive layers is connected to	at least one of the source, gate and drain electrodes of a thin film transistor

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
				one of a plurality of terminals of a thin film transistor."	
	a plurality of terminals of a thin film transistor (C)		the terminals (i.e., source, drain, or gate) of a thin film transistor	this term should be construed as part of the larger term "one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor" to the extent that the embedded term "terminals of a thin film transistor" needs to be construed, CMO proposes the following construction: the gate, source, and drain of a thin film transistor	source, drain and gate electrodes of a thin film transistor
	thin film transistor (C)		A three terminal device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the	A three terminal semi-conductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin- film techniques on an insulating substrate rather than in a single crystal silicon wafer.	field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semi-conductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than in a single crystal silicon wafer.	applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.
Claim 10: A liquid crystal display device comprising:	liquid crystal display device (C)	a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel. [Previously Agreed upon Construction]	a type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel.	A type of display that generates an image by directing light through an array of liquid crystal pixels, where the amount of light effused by each pixel is controlled via an electric field varying the orientation of the liquid crystal molecules contained within the pixel.	plain meaning
a substrate;	Substrate (C)	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support. Previously Agreed upon Construction]	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.

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a first conductive layer on said substrate including: **a gate electrode,** **a gate pad, and** **a source pad;**	Conductive layer (L, C)	See Claim 1 above	See Claim 1 above	See Claim 1 above	See Claim 1 above
	gate electrode (C, A)	"A patterned, electrically conductive material formed over the gate region, current flows through the channel between the source electrode and drain electrode under control of the gate electrode." The court rejects a construction of "electrode" that specifically excludes the line and pad.	a patterned electrically conductive material that controls current flow through the channel between the source electrode and drain electrode	A patterned, electrically conductive material that controls current flow through the channel between the source electrode and drain electrode.	A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode
	gate pad (C, A)	"A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a gate driving circuit."	a portion of patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit.	a patterned, electrically, conductive material that is provided near the periphery of the thin film transistor array to receive a gate signal from a gate driving circuit
	source pad (L, C, A)	"A portion of the patterned electrically conductive material that is provided near the periphery of the thin film transistor array to receive data from a data driving circuit."	a portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal	A portion of patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit.	A patterned, electrically conductive material that is provided near the periphery of the thin film transistor array to receive a data signal from a data driving circuit

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
a gate insulating film on said surface of said substrate,	a gate insulating film on said surface of said substrate (C)		a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor above and in contact with at least part of the surface of the substrate	Plain meaning	A gate insulating film above, supported by, and in contact with the surface of the substrate
	gate insulating film (C)		a thickness of non-conductive material (such as SiNx) that has high electrical resistance and insulates the transistor gate from the semiconductor	Plain meaning	Plain meaning; or Insulating film formed over the gate region
	insulating film (C)	A thickness of non-conductive material (such as SiNx) that has high electrical resistance. [Previously Agreed upon Construction]	a thickness of non-conductive material (such as SiNx) that has high electrical resistance		plain meaning
a portion of said gate insulating film overlying said gate electrode;					
a semiconductor layer on said portion of said gate insulating film;	a semiconductor layer on said portion of said gate insulating film (C)		a thickness of semiconductor material above and in contact with a part of the gate insulating film	a thickness of semiconductor material above and in contact with a part of the gate insulating film	A semiconductor above, supported by, and in contact with the portion of the gate insulating film.
	semiconductor layer (C)	A thickness of a semiconductor material, such as amorphous	a thickness of semiconductor material, such as amorphous	A thickness of a semiconductor material, such as	plain meaning

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		silicon. [Previously Agreed upon Construction]	silicon	amorphous silicon	
an impurity-doped semiconductor layer on said semiconductor layer;	impurity-doped semiconductor layer (C)	A thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have beeo added to enhance electrical conductivity. [Previously Agreed upon Construction]	a thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity	A thickness of semiconductor material, such as amorphous silicon, to which impurities (such as phosphorous atoms) have been added to enhance electrical conductivity.	Plain meaning; or Semiconductor layer doped with impurities
a source electrode and a drain electrode on said semiconductor layer;	a source electrode and a drain electrode on said semiconductor layer (A)		a source electrode and a drain electrode above and in contact with the semiconductor layer	a source electrode and a drain electrode above and in contact with the semiconductor layer	The source electrode and the drain electrode above, supported by, and in contact with the semiconductor layer
	source electrode (C, A)	"A patterned, electrically conductive material formed over the source region, current flows through the channel between the source electrode and drain electrode under control of the gate electrode." The court rejects a construction of "electrode" that specifically excludes the line and pad.	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	Construe term: "a source electrode and a drain electrode" as: Patterned, electrically conductive material formed over the source region and drain region, respectively, of a transistor. Current flows through the channel between the source electrode and	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
				the drain electrode of the transistor under control of the gate electrode of the transistor.	
	drain electrode (C, A)	"A patterned, electrically conductive material formed over the drain region, current flows through the channel between the source electrode and drain electrode under control of the gate electrode."	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source and drain electrode under the control of the gate electrode.	this term should be construed as part of the larger term "a source electrode and a drain electrode" (see above)	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;	passivation layer (C)	A thickness of insulative material that provides protection such as electrical stability and chemical isolation. [Previously Agreed upon Construction]	a thickness of insulative material that provides protection such as electrical stability and chemical isolation	A thickness of insulative material that provides protection such as electrical stability and chemical isolation.	plain meaning
a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad; **a second contact hole provided through said passivation layer exposing said drain electrode;**					
a third contact hole	exposing said gate pad		removing portions of	Plain meaning	Causing the gate pad to be

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
provided through said passivation layer and said gate insulating film exposing said gate pad;	[portion] (A)		one or more layers to uncover at least part of a gate pad [portion]		exposed to the atmosphere
	exposing (C)		removing portions of one or more layers to uncover at least part of another layer	Plain meaning	Laying open or causing to be exposed from above
a fourth contact hole provided through said passivation layer exposing said source electrode;					
a pixel electrode electrically connected with said drain electrode via said second contact hole; and	pixel electrode (C)	a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device. [Previously Agreed upon Construction]	a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device	electrode controlling the brightness of a pixel	Electrode controlling the brightness of a pixel
a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.	transparent conductive layer (C)	A thickness of electrically conductive material. [Previously Agreed upon Construction]	a thickness of transparent electrically conductive material	Plain meaning	plain meaning
	electrically connecting (A)		provide an electrical conduction path	Plain meaning	plain meaning
Claim 11: A method of manufacturing a liquid crystal display device,	a method of manufacturing a liquid crystal display device (C)		a process for producing a liquid crystal display device	Plain meaning	plain meaning

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comprising the steps of:					
forming a first conductive layer on a substrate;	Substrate (C)	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support. Previously Agreed upon Construction]	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
	Conductive layer (L, C)	See Claim 1 above	See Claim 1 above	See Claim 1 above	See Claim 1 above
patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;					
forming an insulating film on said substrate including said patterned conductive layer;					
forming a semiconductor layer on said insulating film;					
forming an impurity-doped semiconductor layer on said semiconductor layer;					
patterning said impurity-doped semiconductor layer	patterning ... to form an active layer (C)		the removal of selected portions of the impurity-doped	Plain meaning	selectively removing portions of … using etching techniques in

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
and said semiconductor layer to form an active layer;			semiconductor layer and the semiconductor layer using etching techniques in order to form an active layer		order to form an active region
	patterning (C)	the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material [Previously Agreed upon Construction]	the removal of selected portions of a surface using etching techniques in order to produce a pattern in the remaining material	Plain meaning	selectively removing portions of a surface using etching techniques in order to produce a pattern in the remaining material
	active layer (C, A)	"A discrete portion of the semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode."	a discrete portion of semiconductor layer that is formed by patterning and located at least in part above the gate electrode. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode.	A discrete portion of the semiconductor layer that is formed by patterning and located along the gate electrode of a thin film transistor. In operation, the discrete portion is penetrated, at least in part, by the electric field introduced by the gate electrode of the thin film transistor.	active region of a thin film transistor
forming a second conductive layer overlying said substrate including said active layer;					
patterning said second conductive layer to					

	U.S. Patent No. 5,825,449 Terms & Limitations	Prior Court Construction	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
form source electrode and a drain electrode on said active layer;					
forming a passivation film overlying said suhstrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;					
selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;	selectively etching (C)		The removing selected portions of a surface using etching techniques (such as wet etching, plasma etching, reactive ion etching, and ion etching) in order to produce a desired pattern on the surface.	Plain meaning	selectively removing portions of a surface using etching techniques in order to produce a desired pattern in the remaining material
patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;	patterning a pixel electrode electrically connected to said drain electrode (C)		the removal of selected portions of a pattern of transparent electrically conductive material to form a pixel electrode that has an electrical conduction path with	Plain meaning	selectively removing portions of a pixel electrode using etching techniques in order to electrically connect the pixel electrode to the drain electrode

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			the drain electrode		
	electrically connected (A)		provide an electrical conduction path	Plain meaning	plain meaning
patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and	electrically connected (A)		provide an electrical conduction path	Plain meaning	plain meaning
patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.	electrically connecting (A)		provide an electrical conduction path	Plain meaning	plain meaning

	U.S. Patent No. 6,664,569 Terms & Limitations	LGD Proposed Construction	AUO Proposed Construction
Claim 17: A liquid crystal display (LCD) device, comprising:			
a substrate;			
a gate line on the substrate and extending along a first direction, the gate line having an opening therein; a first insulating layer on the gate line;	the gate line having an opening therein (A)	the gate line has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment	Gate line with a cut out extending from the periphery of the gate line to the interior of the gate line
	a gate line (L)	a pattern of electrically conductive material that conveys gate signals to transistors, a portion of which controls current flow through the channel between the source and drain electrodes	An elongated directional conductor that supplies signals to gate electrodes
	having an opening therein (L)	has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment	Having a cut out extending from the periphery to a point within
a semiconductor layer on the first insulating layer over at least a portion of the opening; a data line on the insulating layer and extending along a second direction substantially perpendicular to the first direction;	a semiconductor layer on the first insulating layer over at least a portion of the opening (A)	a layer of semiconductor material, above and supported by or in contact with the first insulating layer, a portion of which overlaps art of the space in the gate line	A semiconductor layer above, supported by, and in contact with the first insulating layer, the semiconductor layer being over at least a portion of the opening in the gate line
a drain electrode on the semiconductor layer over at least a portion of the opening; and	a drain electrode on the semiconductor layer over at least a portion of the opening (A)	a drain electrode, above and supported by or in contact with the semiconductor layer, a portion of which overlaps part of the space in the gate line	A drain electrode above, supported by, and in contact with the semiconductor layer, the drain electrode being over at least a portion of the opening in the gate line
	drain electrode (A)	a patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain	A patterned, electrically conductive material formed over the drain region. Current flows through the channel between the source electrode and drain electrode under control of

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		electrode under control of the gate electrode.	the gate electrode.
a source electrode on the semiconductor layer, extending from the data line and being separated and spaced apart from the drain electrode.			
Claim 19: The LCD device to claim 18, further comprising a pixel electrode disposed in a pixel region that is defined by an intersection of the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole.	pixel electrode (A)	a pattern of transparent electrically conductive material that stores charge to drive the liquid crystal material within an individual element of the liquid crystal display device	Electrode controlling the brightness of a pixel
Claim 21: The LCD device of claim 17, wherein the source electrode substantially surrounds the drain electrode.	substantially surrounds the drain electrode (A)	extending considerably around a portion of the drain electrode	Surrounds almost all the drain electrode portion
	Substantially	considerably	Almost all
Claim 25: A liquid crystal display (LCD) device, comprising:			
a substrate;			
a gate line on the substrate and extending along a first direction, the gate line including a gate electrode, the gate electrode having an opening therein, wherein the opening includes a first opening portion and a second opening portion;	the gate electrode having an opening therein (A)	the gate electrode has a space in its pattern to reduce gate-drain capacitance and compensate for gate-drain layer misalignment	gate electrode with a cut out extending from the periphery of the gate line to the interior of the gate line
	gate electrode (L, A)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and the drain electrode under control of the gate electrode.
	the opening includes a first	the space in the gate electrode pattern	Non-rectangular-shaped opening having two

	U.S. Patent No. 6,664,569 Terms & Limitations	LGD Proposed Construction	AUO Proposed Construction
	opening portion and a second opening portion (A)	includes a first part to primarily compensate for gate-drain layer misalignment and a second part to primarily reduce gate-drain capacitance	distinct opening portions
	a first opening portion (L)	a first part to primarily compensate for gate-drain layer misalignment	One distinct opening portion
	a second opening portion (L)	a second part to primarily reduce gate-drain capacitance	Another distinct opening portion
a first insulating layer on the gate line;			
a semiconductor layer on the first insulating layer;			
a data line on the insulating layer and extending along a second direction;			
a drain electrode having a first electrode and a second electrode, the first electrode of the drain electrode overlapping at least a part of the first opening portion of the gate electrode; and	a first electrode (L)	a first portion of the drain electrode to primarily compensate for gate- drain layer misalignment	One distinct portion of a single electrode
	a second electrode (L)	a second portion of the drain electrode to primarily reduce gate-drain capacitance	Another distinct portion of the single electrode
a source electrode on the semiconductor layer, extending from the data line and being separated and spaced apart from the drain electrode.	source electrode (A)	a patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.	A patterned, electrically conductive material formed over the source region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
Claim 32: The liquid crystal display device of claim 25, further comprising a pixel electrode and the drain	a third electrode (L)	a third portion of the drain electrode to primarily connect to the pixel electrode	The third distinct portion of the single electrode

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electrode further comprising a third electrode contacting the pixel electrode.			
Claim 34: The liquid crystal display device of claim 32, wherein the second electrode of the drain electrode connects the first and third electrodes of the drain electrodes.	Connects (L)	joins	physically attached

	U.S. Patent No. . 6,803,984 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1: A method for manufacturing a liquid crystal display device, comprising the steps of:	a liquid crystal display device (C)			
providing at least a first substrate and a second substrate on a single production process line;	a first substrate and a second substrate on a single production process line (C)			
	a first substrate (C)	one of a TFT or color filter substrate	Plain meaning	Plain meaning; Or one of the two opposing substrates of the liquid crystal cell
	a second substrate (C)	the other of the TFT or color filter substrate	The substrate immediately following the first substrate	Plain meaning Or the other of the two opposing substrates of the liquid crystal cell
	on a single production process line (L)	on a production line where the processing equipment is arranged along a common path for performing the liquid crystal cell processes	On a line structure for processing the substrates in only one direction without branching	On a production line for processing liquid crystal displays in a single, linear arrangement

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passing the first and second substrates through a sealing material coating portion of the single production process line in serial order,	passing the first and second substrates through a sealing material coating portion... in serial order (C)	passing the first and second substrates, one after the other, along a portion of the single production process line where the sealing material is selectively applied	Providing the first and second substrates, one after the other without anything in between, in at one end, of a machine for coating sealing material in the single production process line in which the same order of the first and second substrates is maintained throughout the seal dispensing process	providing the first and second substrates one after the other, without anything in between; in at one end, and out at the other end in the same order of an equipment/machine[2] for coating sealing material on a substrate in the single production process line
	a sealing material coating portion of the single production process line (A)	a portion of the single production process line where the sealing material is selectively applied	a machine for coating sealing material in the single production process line	An equipment/machine[3] for coating sealing material in the single production process line.
	in serial order (A)	one after the other	one after the other one without anything in between	One after the other without anything in between
a sealing material being coated on the second substrate with the first substrate being passed through the sealing material coating portion without forming a sealing material thereon;				
passing the first and the second substrates through a liquid crystal dispensing portion of the single production process line in	passing the first and second substrates through a liquid crystal dispensing portion of the single production process line in serial order	passing the first and second substrates, one after the other, along a portion of the single production process line where liquid crystal is selectively	providing the first and second substrates, one after the other without anything in between, in at one end, and out at the other end, of a machine for dispensing	providing the first and second substrate one after the other, without anything in between; in at one end, and out at the other end in the same order of

[2] Due to a clerical error, the word "equipment" as inadvertently omitted from the previously submitted JCC. It is reinserted herein.

[3] The word "equipment" was inadvertently omitted from the previously submitted JCC due to clerical error.

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serial order, liquid crystal being dispensed onto a pixel region of one of the first and second substrates with the other one of the first and second substrates being passed through the liquid crystal dispensing portion without dispensing liquid crystal thereon; and	(C)	dispensed	liquid crystal material in the single production process line in which the same order of the first and second substrates is maintained throughout the liquid crystal dispensing process	the liquid crystal dispensing machine/equipment[4]
	a liquid crystal dispensing portion of the single production process line (A)	a portion of the single production process line where liquid crystal is selectively dispensed	a machine for dispensing liquid crystal in the single production process line	an equipment/machine[5] for dispensing liquid crystal on a substrate in the single production process line
	a pixel region (C)	area corresponding to the inside of the sealing material	an area with pixels	Area with pixel
assembling the first substrate with the second substrate to form a liquid crystal panel of at least one liquid crystal display device.	assembling (C)	bring together	Indefinite	Indefinite
Claim 5: The method according to claim 4, wherein the first substrate is disposed in the liquid crystal dispensing portion and the liquid crystal is dispensed onto the first substrate at the same time that the second substrate	the liquid crystal is dispensed onto the first substrate at the same time that the second substrate is disposed in the sealing material coating portion (A)	a point in time when liquid crystal is being dispensed on the first substrate overlaps with a point in time when the second substrate is located in the portion of the single production process line where the sealing material is selectively applied	when the liquid crystal is dispensed onto the first substrate in the machine for dispensing liquid crystal, the second substrate is located in the machine for coating sealing material	when the liquid crystal is dispensed onto the first substrate in the liquid crystal dispensing machine, the second substrate is located in the sealant coating machine

(...continued)

[4] The word "equipment" was inadvertently omitted from the previously submitted JCC due to clerical error.

[5] The word "equipment" was inadvertently omitted from the previously submitted JCC due to clerical error.

	U.S. Patent No. . 6,803,984 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
is disposed in the sealing material coating portion.				
Claim 10: The method according to claim 1, further comprising the step of cleaning the first substrate and the second substrate in serial order in a same cleaning unit.	in serial order in a same cleaning unit (L)	one after the other in the same cleaning equipment	one after the other without anything in between, in a same cleaning machine	cleaning the first substrate and the second substrate one after the other without anything in between in the same cleaning machine

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1: A thin film transistor comprising:	transistor (C)	a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate	a three terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate electrode, which is separated from the semiconductor by an insulating layer, and the thin film transistor is formed using thin-film techniques on a substrate	Plain meaning Or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate
a substrate; and	substrate (C)	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second	gate (L)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A region of a transistor.	same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than the second metal layer by about 1 to 4 μm.				electrode under control of the gate electrode.
	[a] double-layered structure (C, A)	[a] structure of an electrically conductive material that includes two sequentially deposited metal layers	A structure having only two metal layers.	a two-layered step structure
	[a] second metal layer disposed on the first metal layer (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is in contact with the first metal layer.	a second metal layer precipitated above, supported by and in contact with the first metal layer
	the first metal layer including aluminum (C)	the first metal layer containing aluminum and possibly other materials	plain meaning	plain meaning
	the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer (C)	the second metal layer is patterned to prevent hillock on the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer	The second metal layer prevents hillock on the sides of the aluminum first metal layer.	the second metal layer being arranged on the first metal layer to prevent hillocks from forming on the side portions of the aluminum first metal layer
	[at] the sides of the aluminum first metal layer (L, C, A)	the side surfaces of the first metal layer that are exposed to a subsequently deposited gate insulating layer	Indefinite.	at the portions on the top surface of the first metal layer not covered by the second metal layer
	[the] first metal layer being wider than the second metal layer by about 1 to 4 μm (L, C, A)	the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1μm and less than 4μm greater than the width of the second metal layer	The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second	Indefinite; or the first metal layer is about 1 to 4 μm greater than the width of the second metal layer measured from a level defined by the top of the first metal

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
			metal layer.	layer
Claim 2: The thin-film transistor as claimed in claim 1, wherein the second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second metal layer disposed thereon have the same width as each other.	two side portions of the first metal layer having no second layer disposed thereon	the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	the two side portions on the top surface of the first metal layer not covered by the second layer
Claim 4: A thin film transistor comprising:	transistor (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
a substrate;	substrate (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
a gate including a double-layered structure having a first metal layer which is a bottom layer disposed on the substrate and a second metal layer disposed on the first metal layer, the first metal layer including aluminum, the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer, the first metal layer being wider than	gate (L)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	[a] double-layered structure (C, A)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	[a] second metal layer disposed on the first metal layer (L, C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	the first metal layer including aluminum (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	the second metal layer being arranged on the first metal layer to prevent hillock at the sides of the aluminum first metal layer (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above
	[at] the sides of the aluminum first metal layer (L, C, A)	See Claim 1 above	See Claim 1 above	See Claim 1 above

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
the second metal layer by about 1 to 4 μm;	[the] first metal layer being wider than the second metal layer by about 1 to 4 μm (L, C, A)	See Claim 1 above	See Claim 1 above	See Claim 1 above
a first insulating layer disposed on the substrate including the gate;				
a semiconductor layer disposed on a portion of the first insulating layer at a location corresponding to the gate;				
an ohmic contact layer disposed on two sides of the semiconductor layer;				
a source electrode and a drain electrode disposed on the ohmic contact layer and extending onto the first insulating layer; and				
a second insulating layer covering the semiconductor layer, the source and drain electrodes and the first insulating layer.				
Claim 5: The thin-film transistor as claimed in claim 1, wherein the	two side portions of the first metal layer having no second layer thereon (C)	See Claim 1 above	See Claim 1 above	See Claim 1 above

	U.S. Patent No. 5,905,274 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
second metal layer is located in a middle portion of the first metal layer so that two side portions of the first metal layer having no second metal layer disposed thereon have the same width as each other.				

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 7: A method of forming a thin film transistor comprising:	transistor (C)	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate	Plain meaning Or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate
forming a first metal layer on a substrate,	substrate (C)	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	plain meaning
forming a second metal layer on the first metal layer;	forming a second metal layer on the first metal layer (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is formed in direct contact with the first metal layer.	forming a second metal layer above, supported by, and in contact with the first metal layer
simultaneously patterning the first and second metal layers to	[a] double-layered metal gate (C, A)	[a] patterned structure of an electrically conductive material that includes two sequentially deposited	A double-layered metal gate is a gate having only two metal layers.	a gate electrode having a two-layered step structure

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
form a double-layered metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.		metal layers and includes a portion that controls current flow through the channel between the source electrode and drain electrode		
	gate (L)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A region of a transistor.	same as gate electrode; a patterned, electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode.
	[a] total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm (L, C, A)	the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4μm greater than the width of the second metal layer	The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.	Indefinite; or the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer
Claim 7: A method of forming a thin film transistor comprising: forming a first metal layer on a substrate, forming a second metal layer on the first metal layer; simultaneously patterning the first and second metal layers to form a double-layered	simultaneously patterning (A)	removing part of the first and second metal layers during a single etching process	Plain meaning	Forming the patterned first and second metal layers at the same time in one chemical etching step

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
metal gate, so that a total width of the first metal layer is greater than a total width of the second metal layer by about 1 to 4 μm.				
Claim 8: The method of claim 7, wherein the first and second metal layers are patterned so that the first metal layer has a first and a second side portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.	a first and a second side portion being exposed from the second metal layer (C)	first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	A first side portion and a second side portion on the top surface of the first metal layer not covered by the second layer
Claim 10: The method of claim 7, wherein the patterning step is such that the second metal layer is etched faster than the first etching layer.	first etching layer (L)	the first metal layer	Indefinite.	indefinite
Claim 16: A method of waking a thin-film transistor, comprising the steps of:	transistor (C) Waking (L)	See Claim 7 above making	See Claim 7 above Indefinite.	See Claim 7 above non-sensical; indefinite

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
depositing a first metal layer on a substrate, the first metal layer including aluminum;	the first metal layer including aluminum (C)	the first metal layer containing aluminum and possibly other materials	A first metal layer that includes pure aluminum.	plain meaning
depositing a second metal layer on the first metal layer without forming a photoresist on the first metal layer beforehand;	depositing a second metal layer on the first metal layer (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is deposited in direct contact with the first metal layer.	Precipitating a second metal layer above, supported by, and in contact with the first metal layer
forming a single photoresist having predetermined width on the second metal layer;	forming a single photoresist having a predetermined width on the second metal layer (C) Photoresist (C)	forming a pattern of single photosensitive material that has a specified width on the second metal layer pattern of a photosensitive material	The photoresist is deposited in direct contact with the second metal layer. An etching mask.	plain meaning plain meaning
patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask, the first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm; and removing the photoresist.	simultaneously in a single etching step using the single photoresist as a mask (L)	during a single etching process with a common mask	The first and second metal layers are simultaneously etched in a single step using the photoresist as a mask.	Construe term: "patterning the first and second metal layers simultaneously in a single etching step using the single photoresist as a mask" as forming the patterned first and second metal layers in one chemical etching step using one photoresist mask

	U.S. Patent No. 6,815,321 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
	patterning ... simultaneously (A)	Removing part of the first and second metal layers during a single etching process	Plain meaning	forming the patterned first and second metal layers in one chemical etching step
	[the] first metal layer being etched to have a width greater than a width of the second metal layer by about 1 to 4 μm (L, C, A)	the first and second metal layers are etched such that the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4μm greater than the width of the second metal layer	The first metal layer being etched so that a top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a structure where not all of the top surface of the first metal layer is covered by the second metal layer.	indefinite; or the first metal layers being etched so that the width of the first metal layer is about 1 to 4 μm greater than the width of the second metal layer when measured from a level defined by the top of the first metal layer
Claim 22: The method of making a thin film transistor as claimed in claim 16, wherein two side portions of the first metal layer having no second metal layer deposited thereon have substantially the same width as each other.	two side portions of the first metal layer having no second metal layer deposited thereon (C, A)	the side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning.	The two portions on the top surface of the first metal layer not covered by the second metal layer

	U.S. Patent No. 7,176,489 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1. A thin film transistor comprising:	transistor (C)	A three-terminal semiconductor device in which the current flow through one pair of terminals, the source and drain, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third terminal, the gate, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate rather than a single crystal silicon wafer.	A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulatmg substrate	Plain meaning Or A three-terminal semiconductor device in which the current flow through one pair of electrodes, the source electrode and drain electrode, is controlled or modulated by an electric field that penetrates the semiconductor; this field is introduced by a voltage applied at the third electrode, the gate electrode, which is separated from the semiconductor by an insulating layer. The thin-film transistor is formed using thin-film techniques on an insulating substrate
a substrate; and	Substrate (C)	the material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support	Plain meaning; Or The material (such as glass) upon which a transistor or integrated circuit is fabricated to provide mechanical support.
a double-layered metal gate having a first metal layer and a second metal layer thereon, a total width of the first metal	[a] double layered metal gate (C, A)	[a] patterned structure of an electrically conductive material that includes two sequentially deposited metal layers and includes a portion that controls	A gate having only two metal layers.	A gate electrode having a two-layered step structure

	U.S. Patent No. 7,176,489 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
layer being greater than a total width of the second metal layer by about 1 to 4 μm.		current flow through the channel between the source electrode and drain electrode		
	gate (L)	patterned electrically conductive material that includes a portion that controls current flow through the channel between the source electrode and drain electrode	A region of a transistor.	same as gate electrode; a patterned electrically conductive material formed in the gate region. Current flows through the channel between the source electrode and drain electrode under control of the gate electrode
	[having] a first metal layer and a second metal layer thereon (L, C)	sequentially depositing the second metal layer above and in contact with the first metal layer	The second metal layer is in contact with the fast metal layer.	The double layered metal gate having a first metal layer and a second metal layer formed on the top surface of the first metal layer
	a total width of the first metal layer being greater than a total width of the second metal layer by about 1 to 4 μm (L, C, A)	the width of the first metal layer, determined by the portion of the first metal layer in contact with the second metal layer together with the portions exposed to the subsequently deposited gate insulating layer, is more than 1 μm and less than 4μm greater than the width of the second metal layer	The top surface of the first metal layer has a width that is about 1 to 4 μm wider than a width of the top surface of the second metal layer to form a double step. A double step is a gate where not all of the top surface of the first metal layer is covered by the second metal layer.	Indefinite; or The width of the first metal layer is about 1 to 4 μm greater than the width of the second metal measured from a level defined by the top of the first metal layer
Claim 2. The transistor of claim 1, wherein the first metal layer has a first and second side portion being exposed from the second metal layer, each side portion being at least about 0.5 μm in width.	a first and second side portion being exposed from the second metal layer (C, A)	first and second side surfaces of the first metal layer that are exposed to the subsequently deposited gate insulating layer	Plain meaning	The two side portions on the top surface of the first metal layer not covered by the second metal layer

	U.S. Patent No. 7,176,489 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 3. The transistor of claim 2, wherein each side portion of the first metal layer is less than about 2 μm in width.	side portion of the first metal layer (A)	side surface of the first metal layer exposed to the subsequently deposited gate insulating layer	Plain meaning	*Construed with "each" in front:* Each of the first and second side portions on the top surface of the first metal layer not covered by the second metal layer

	U.S. Patent No. 7,218,374 Terms & Limitations	LGD Proposed Construction	CMO Proposed Construction	AUO Proposed Construction
Claim 1: A method of manufacturing a liquid crystal display (LCD) device comprising:				
preparing a lower substrate and an upper substrate;	preparing a lower substrate and an upper substrate (C)	making the substrates ready for depositing sealant and liquid crystal material prior to attachment	indefinite	indefinite
forming an auxiliary sealant and subsequently forming a main sealant on one of the lower and upper substrates, wherein the auxiliary sealant is formed in a dummy region and connects to the main sealant, and wherein the auxiliary sealant and the main sealant are contiguous;	forming a main sealant (L)	depositing sealant material that encloses the display region	Forming sealing material necessary for confining liquid crystal from leaking out from between the substrates.	forming a segment of sealant that encloses the liquid crystal in the LCD panel
	main sealant (C, A)	sealant material that encloses the display region	sealant material necessary for confining liquid crystal from leaking out from between the substrates	a segment of sealant for enclosing the liquid crystal in the LCD panel
	auxiliary sealant (C, A)	sealant deposited in an area outside of the main sealant	sealant material that is not necessary for confining liquid crystal from leaking out from between the substrates	A segment of sealant that extends from the main sealant and is outside the enclosure of the main sealant
	[a] dummy region (L, A)	an area outside of the main sealant	an area outside the boundary of the main sealant	An area outside the enclosure of the main sealant
	connects to the main sealant (L)	joined to the main sealant	physically attached to the main sealant	Physically attached to the main sealant
	wherein the auxiliary sealant and the main sealant are contiguous (L, C, A)	wherein the auxiliary and main sealants are deposited in a continuous process	wherein the auxiliary sealant touches but does not overlap the main sealant	Wherein the auxiliary sealant and the main sealant are physically connected to each other

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applying a liquid crystal on one of the lower and upper substrates;	applying a liquid crystal on one of the lower and upper substrates (L, C, A)	depositing the liquid crystal onto either one of the substrates	Plain meaning.	plain meaning
attaching the lower and upper substrates; and	attaching the lower and upper substrates (A)	pressing the lower and upper substrates together	putting the lower and upper substrates together as one single piece	Putting the lower and upper substrates together as one single piece
curing at least the main sealant.				
Claim 2: The method of claim 1, wherein the main sealant and the auxiliary sealant are at least partially curable by irradiating UV light and curing the main sealant includes irradiating UV light.				
Claim 5: The method of claim 2, wherein the sealant is formed using oligomers each having one end coupled to an acrylic group and the other end coupled to an epoxy group.				
Claim 10: The method of claim 2, wherein a region where the sealant is not formed is covered with a mask during the irradiating with UV light.				
Claim 11: The method of claim 2, wherein a region				

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where the main UV sealant is not formed is covered with a mask during the irradiating with UV light.				
Claim 16: The method of claim 1, further comprising cutting the attached substrates.				
Claim 17: The method of claim 16, wherein the attached substrates are cut across a portion of the auxiliary sealant.				
Claim 21: A method of manufacturing a liquid crystal display (LCD) device comprising:				
preparing a lower substrate and an upper substrate;				
forming an auxiliary UV sealant and a main UV sealant on one of the lower and upper substrates, wherein the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant, wherein the auxiliary UV sealant contacts the main UV sealant;	forming a main UV sealant (L)	The combination of the construction for "forming a main sealant" with the agreed construction of "UV sealant"		
	main UV sealant (C, A)	The combination of the construction for "main sealant" with the agreed construction of "UV sealant"		
	UV sealant (C)	sealant material that is at least partially curable by UV light	sealant material that is at least partially curable by UV light	sealant material that is at least partially curable by UV light
	[wherein] the auxiliary UV sealant is formed in a dummy region and extends outside from the main UV sealant (L, C, A)	wherein the auxiliary UV sealant is deposited in an area that is outside of the main UV sealant and is joined to the main UV sealant	The auxiliary UV sealant is applied in the outer, non-active region of the substrate beginning from the main UV sealant and moving outward.	Wherein the auxiliary UV sealant is formed in an area outside the enclosure of the main UV sealant
	auxiliary UV sealant (C,	UV sealant deposited in an		a segment of UV sealant that

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	A)	area outside of the main UV sealant		extends from the main sealant but not used to enclose liquid crystal in the finished LCD panel
	[wherein] the auxiliary UV sealant contacts the main UV sealant (C, A)	[wherein] the auxiliary UV sealant touches the main UV sealant	The auxiliary UV sealant touches the main UV sealant.	wherein the auxiliary sealant and the main sealant are physically connected together
applying a liquid crystal on one of the lower and upper substrates;				
attaching the lower and upper substrates; and				
irradiating UV light on the attached substrates.				